EVB Schematics For RK3568

RK_EVB1_RK3568_DDR4P216SD6_V1.0

Main Functions Introduction

1) PMIC: RK809-5+DiscretePower
2) RAM: DDR4 2x16Bit
3) ROM: eMMC5.1+SPI Falsh,Option Nand Flash
4) Support: Micro SD Card3.0
5) Support: 1 x USB3.0 OTG + 1 x USB3.0 HOST + 2 x USB2.0 HOST
6) Support: 1 x SATA3.0 Connector (7pin) + 4 pin Power Connector
7) Support: 1 x 2Lanes PCIe3.0 Connector (RC Mode)
8) Support: 1 x 4Lanes MIPI CSI Camera or 2 x 2Lanes MIPI CSI Camera
9) Support: Parallel CIF Connector(Option-Ext Board)
10) Support: 1 x HDMI2.0 TX
11) Support: eDP to VGA TX or 1 x 4Lanes eDP with Touch Connector(Option)
12) Support: 2 x 4Lanes MIPI DSI or 1 x 4Lanes MIPI DSI + 1 x LVDS with Touch Connector
13) Support: a/b/g/n/ac 2X2 WIFI,BT5.0
14) Support: 2 x 10/100/1000 Ethernet(RGMII)
15) Support: IR Receiver
16) Support: Optical S/PDIF TX
17) Support: Headphone output,1 x ECM MIC and Speaker out(1.3W@8ohm)
18) Support: Array MIC Connector(Ext Board PDM)
19) Support: Gyroscope+G-sensor
20) Support: Array Key(MENU,VOL+,VOL-,ESC),Reset,Power on/off Key
21) Support: 3 x UART + 2 x UART(Option)
22) Support: 1 x CAN FD
23) Support: 5 x SARADC
24) Support: Debug UART to USB connector and JTAG Connector

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File:	00.Cover Page				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
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Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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File:	01.Index and Notes				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
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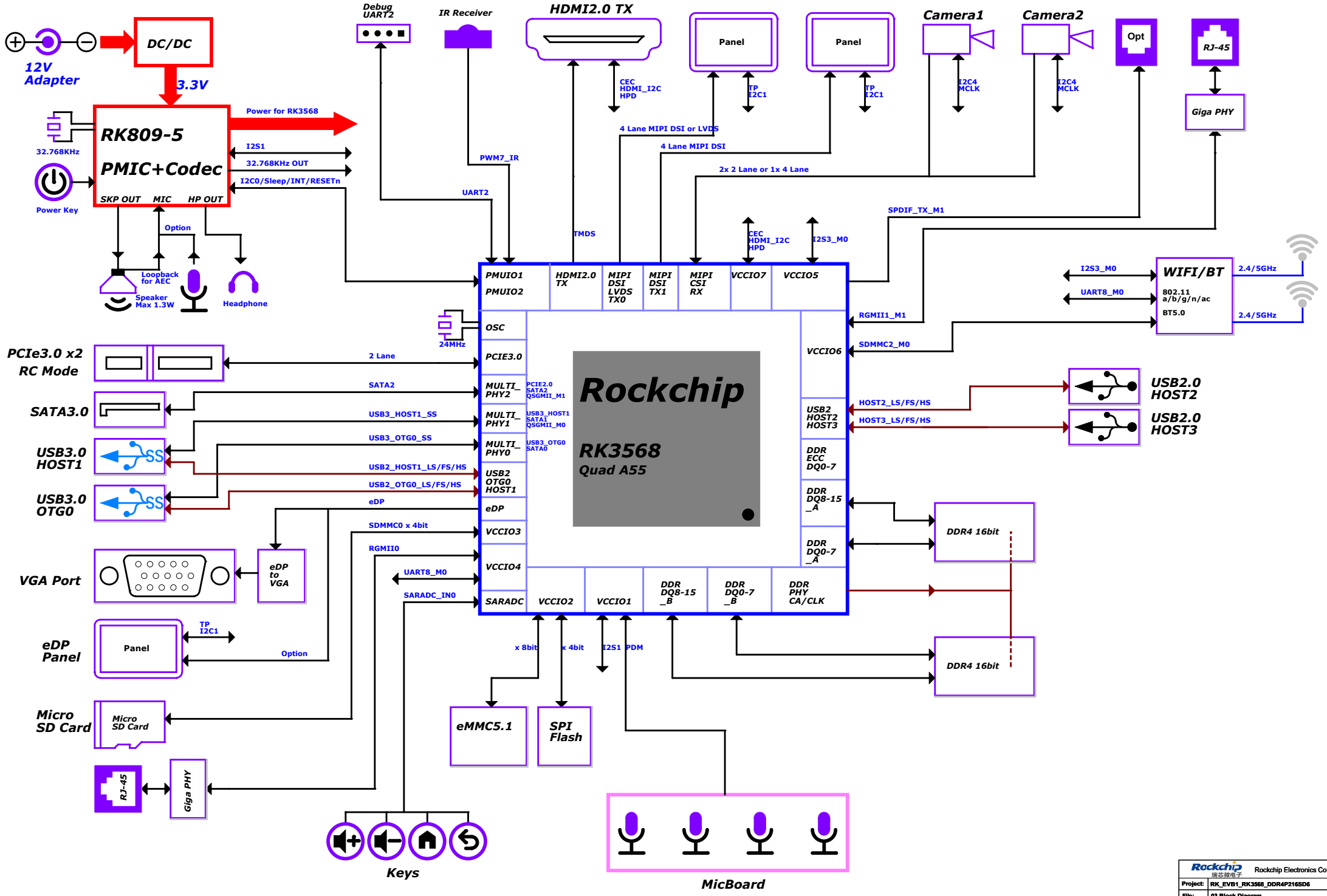
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2020-09-08	Zhangdz	1:Revision preliminary version	

RK3568 Ref Block Diagram



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File:	03.Block Diagram
Date:	Wednesday, September 23, 2020
Rev:	V1.0
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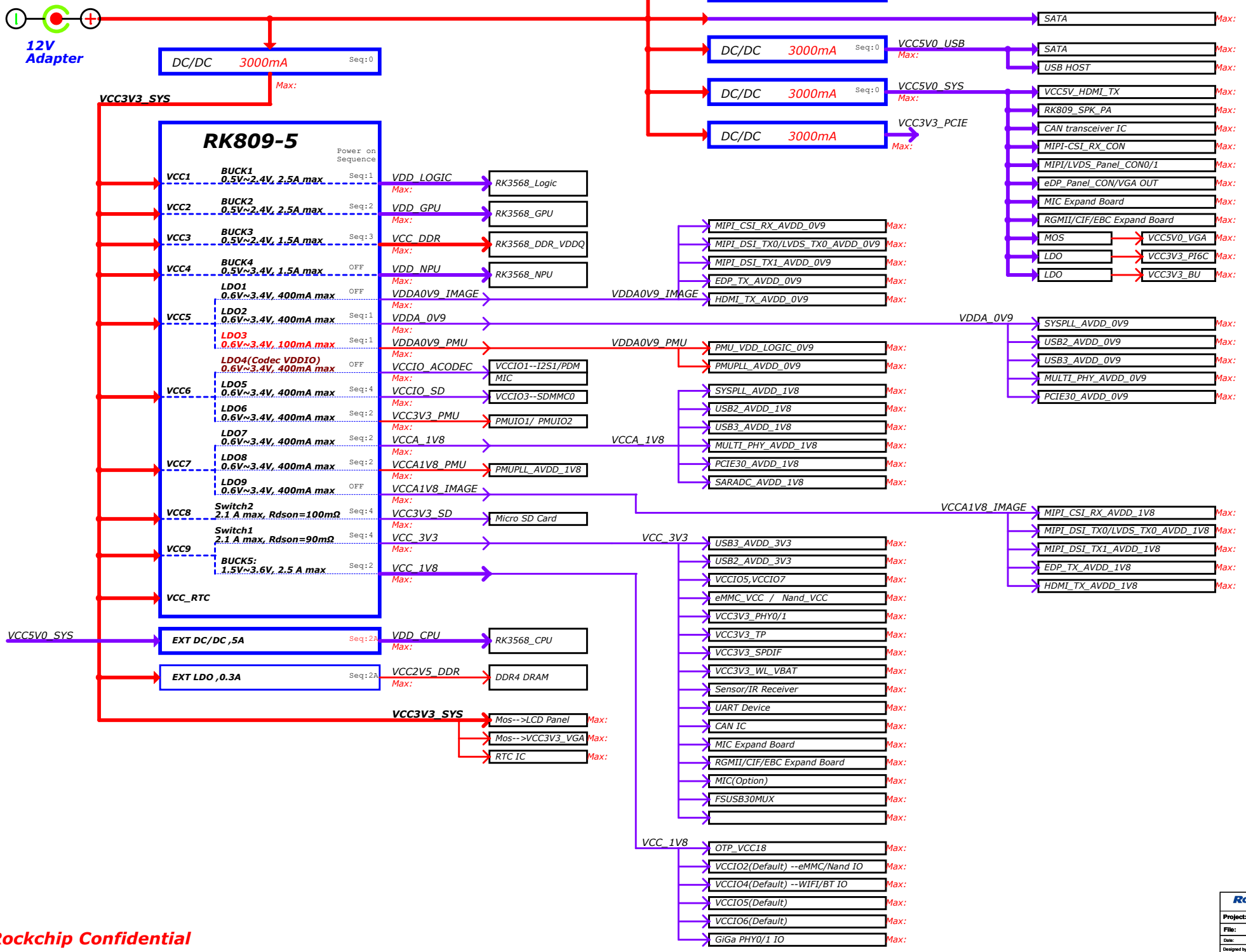
Power Diagram



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File:	04.Power Diagram
Date:	Wednesday, September 23, 2020
Rev:	V1.0
Designed by:	Zhangtz
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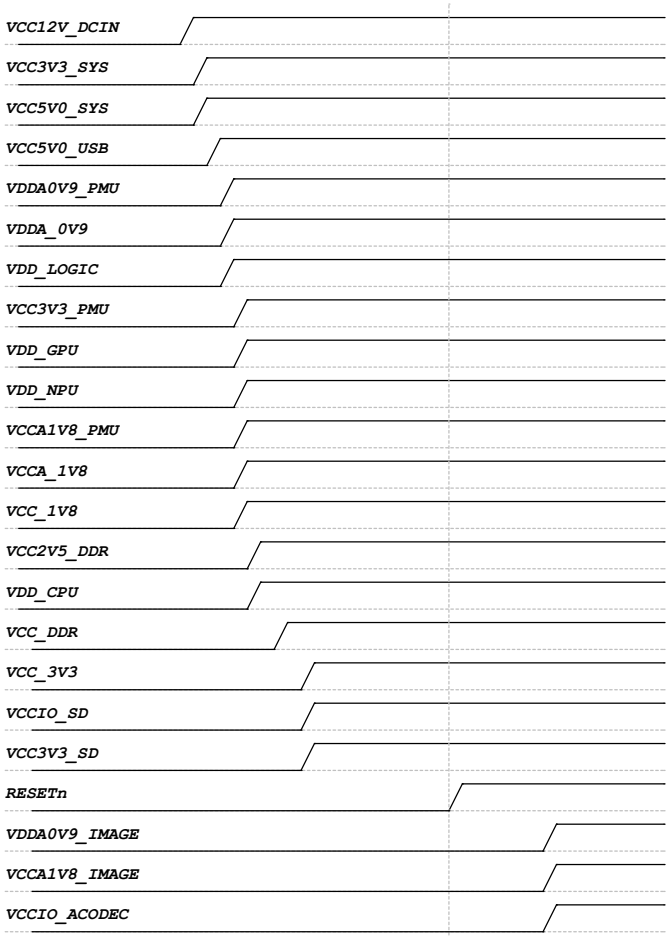
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0.9V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0.9V	OFF	OFF	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	OFF	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	3.3V	OFF	OFF	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	ON	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	ON	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	1.8V	OFF	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	OFF	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	OFF	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	OFF	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	ON	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	OFF	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	OFF	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	ON	TBD	TBD

IO Power Domain Map

Updates must be Revision accordingly!

IO Domain	Pin Num	Support IO Voltage		Actual assigned IO Domain Voltage			Notes
		3.3V	1.8V	Supply Power Net Name	Power Source	Voltage	
PMUIO1	Pin Y20	✓	✗	VCC3V3_PMU	VCC3V3_PMU	3.3V	
PMUIO2	Pin W19	✓	✓	VCC3V3_PMU	VCC3V3_PMU	3.3V	
VCCIO1	Pin H17	✓	✓	VCCIO_ACODEC	VCCIO_ACODEC	3.3V	
VCCIO2	Pin H18	✓	✓	VCCIO_FLASH	VCC_1V8	1.8V	PIN "FLASH_VOL_SEL" must be logic High if VCCIO_FLASH=3.3V,FLASH_VOL_SEL must be logic low
VCCIO3	Pin L22	✓	✓	VCCIO_SD	VCCIO_SD	3.3V	
VCCIO4	Pin J21	✓	✓	VCCIO4	VCC_1V8	1.8V	
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5	VCC_3V3	3.3V	
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6	VCC_1V8	1.8V	
VCCIO7	Pin V12	✓	✓	VCCIO7	VCC_3V3	3.3V	

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File:	05.Power Sequence/IO Domain Map				
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UART MAP

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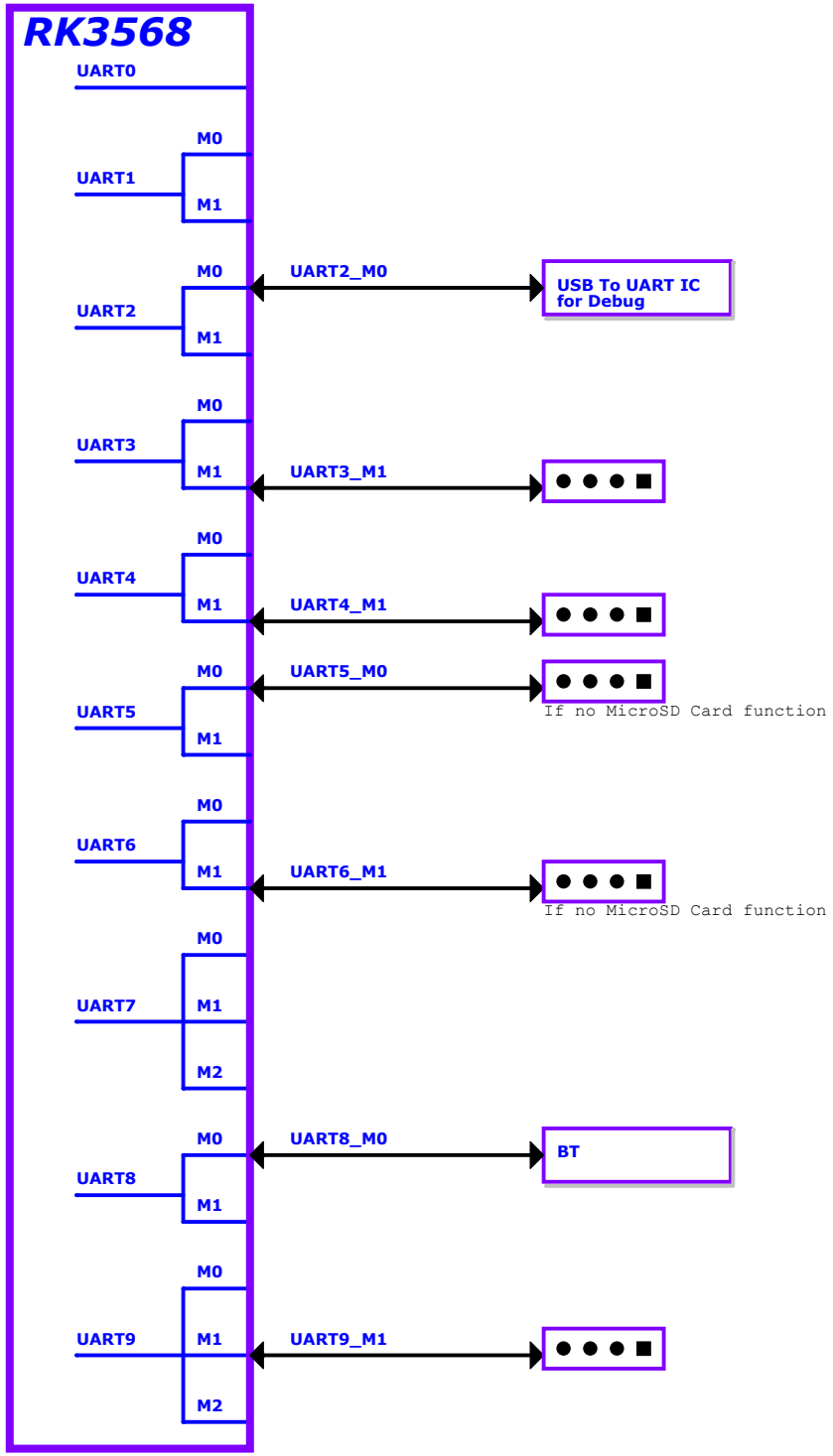

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File:	06.UART Map				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
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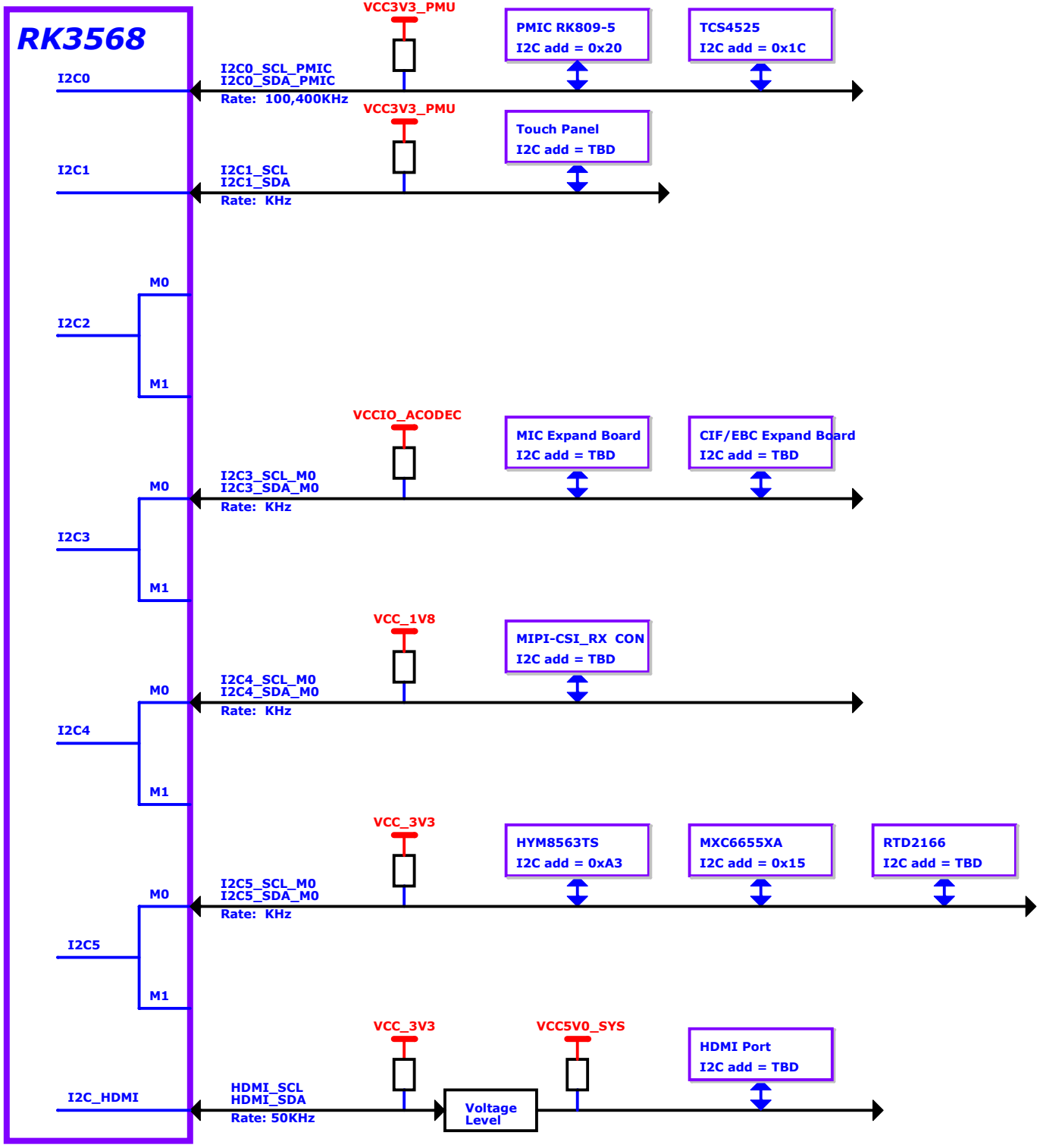
I2C MAP



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Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	07.I2C Bus Map				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
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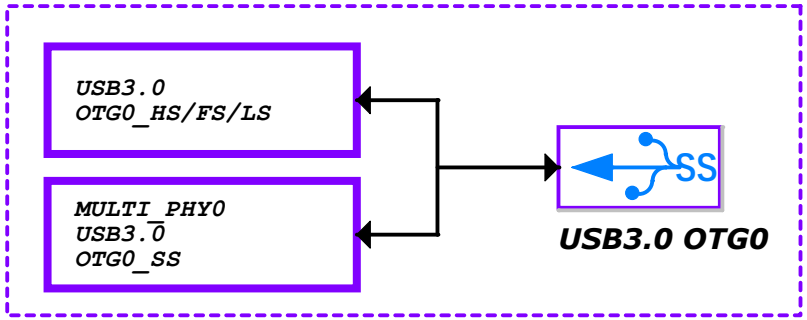
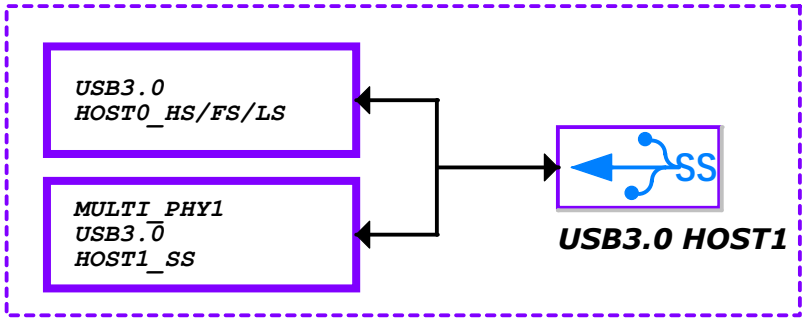
USB3.0 OTG0



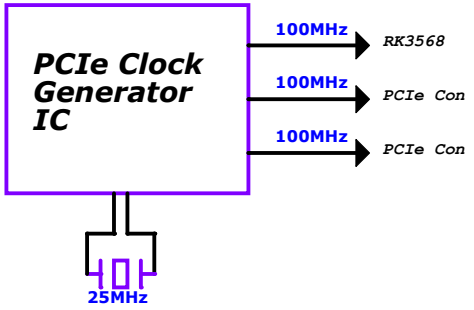
USB3.0 HOST1



PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIE30_REFCLK (RC:input)	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
			PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

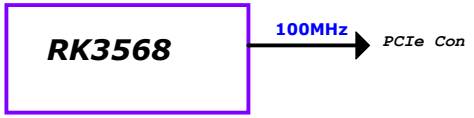
PCIe3.0 REFCLK



PCIe2.0 PHY

MULTI_ PHY2	PCIe2.0 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

PCIe2.0 REFCLK



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Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	08.USB3/PCIE30 Fun Map				
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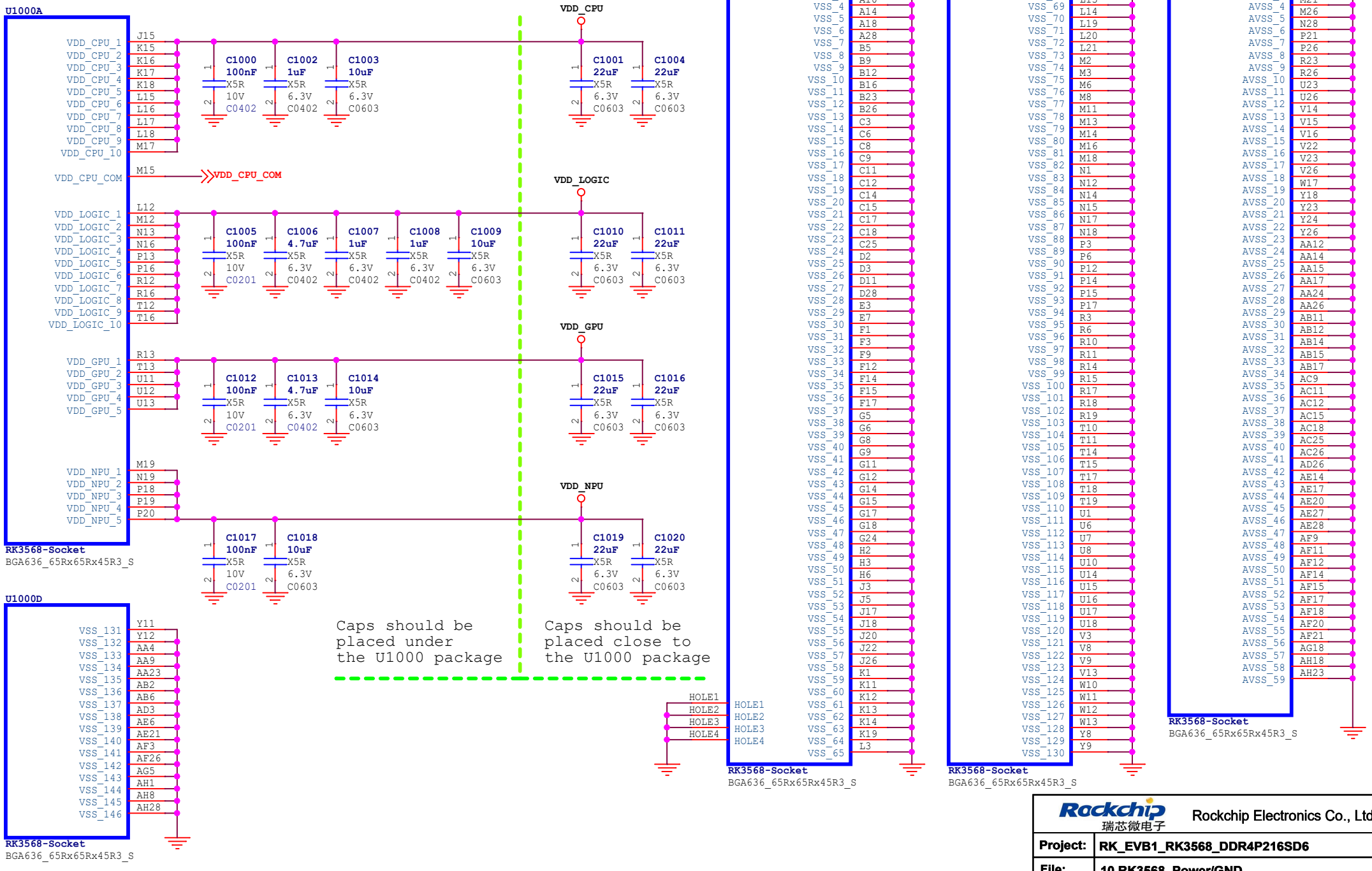
RK3568_ABCDE (Power&Gnd)



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Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	10.RK3568_Power/GND				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
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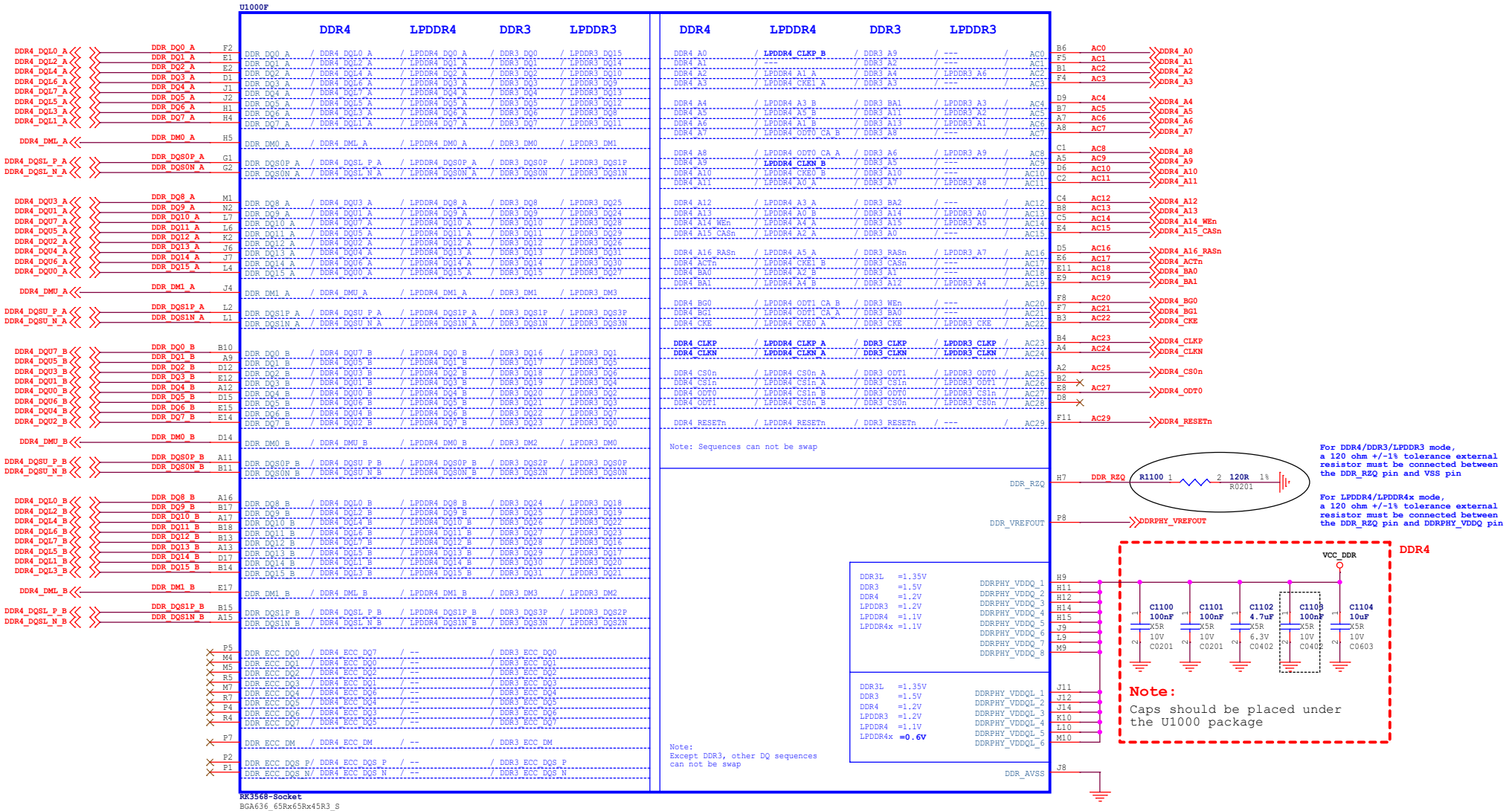
RK3568_F (DDR PHY)



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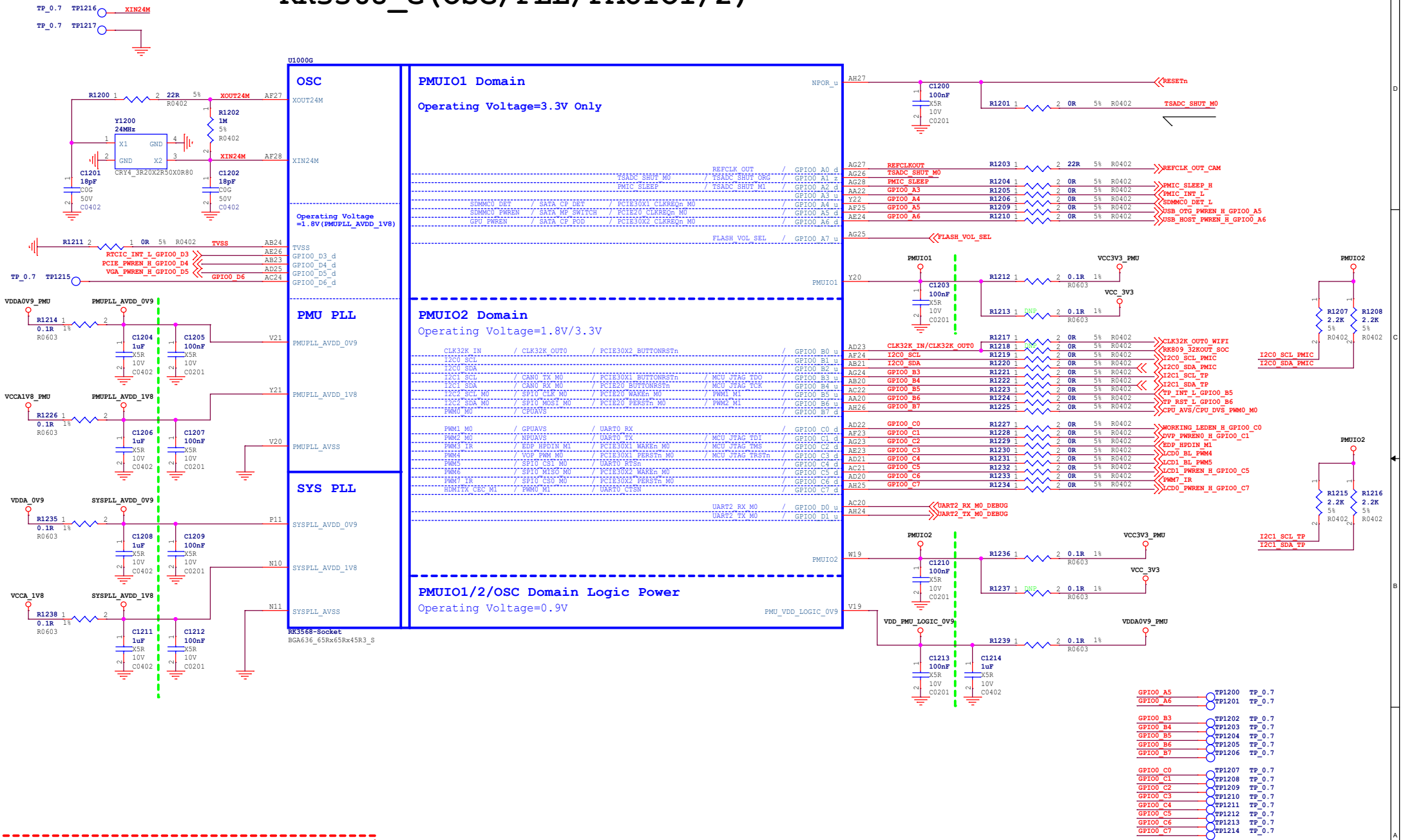
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	11.RK3568_DDR PHY				
Date:	Sunday, September 27, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	11 of 50

RK3568_G(OSC/PLL/PMUIO1/2)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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Project:	RK_EVB1_RK3568_DDR4P216SD6		
File:	12.RK3568_OSC/PLL/PMUIO		
Date:	Wednesday, September 23, 2020	Rev:	V1.0
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RK3568_I(VCCIO2 Domain)

U1000I

VCCIO2 Domain

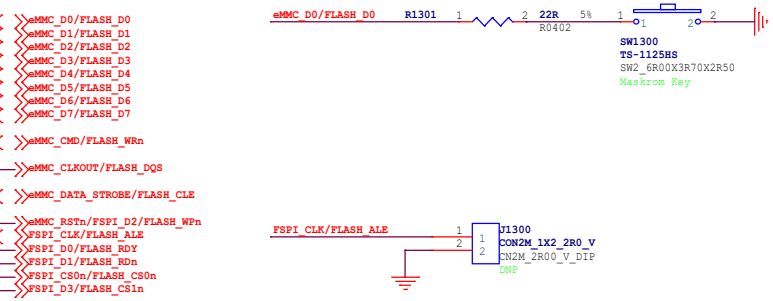
Operating Voltage=1.8V/3.3V

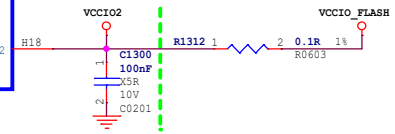
EMMC_D0	/ FLASH_D0	/ GPIO1_B4_u	A24	eMMC_D0/FLASH_D0_SOC	R1300	eMMC_D0/FLASH_D0
EMMC_D1	/ FLASH_D1	/ GPIO1_B5_u	C21	eMMC_D1/FLASH_D1_SOC	R1302	eMMC_D1/FLASH_D1
EMMC_D2	/ FLASH_D2	/ GPIO1_B6_u	B24	eMMC_D2/FLASH_D2_SOC	R1303	eMMC_D2/FLASH_D2
EMMC_D3	/ FLASH_D3	/ GPIO1_B7_u	D21	eMMC_D3/FLASH_D3_SOC	R1304	eMMC_D3/FLASH_D3
EMMC_D4	/ FLASH_D4	/ GPIO1_C0_u	A25	eMMC_D4/FLASH_D4_SOC	R1305	eMMC_D4/FLASH_D4
EMMC_D5	/ FLASH_D5	/ GPIO1_C1_u	E21	eMMC_D5/FLASH_D5_SOC	R1306	eMMC_D5/FLASH_D5
EMMC_D6	/ FLASH_D6	/ GPIO1_C2_u	E22	eMMC_D6/FLASH_D6_SOC	R1307	eMMC_D6/FLASH_D6
EMMC_D7	/ FLASH_D7	/ GPIO1_C3_u	B25	eMMC_D7/FLASH_D7_SOC	R1308	eMMC_D7/FLASH_D7
EMMC_CMD	/ FLASH_WRn	/ GPIO1_C4_u	B22	eMMC_CMD/FLASH_WRn_SOC	R1309	eMMC_CMD/FLASH_WRn
EMMC_CLKOUT	/ FLASH_DQS	/ GPIO1_C5_d	A23	eMMC_CLKOUT/FLASH_DQS_SOC	R1310	eMMC_CLKOUT/FLASH_DQS
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/ GPIO1_C6_d	A26			eMMC_DATA_STROBE/FLASH_CLE
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/ GPIO1_C7_d	F20			eMMC_RSTn/FSPI_D2/FLASH_WPn
	FSPI_CLK / FLASH_ALE	/ GPIO1_D0_d	A22	FSPI_CLK/FLASH_ALE_SOC	R1311	FSPI_CLK/FLASH_ALE
	FSPI_D0 / FLASH_RDY	/ GPIO1_D1_u	C24			FSPI_D0/FLASH_RDY
	FSPI_D1 / FLASH_RDn	/ GPIO1_D2_u	D23			FSPI_D1/FLASH_RDn
	FSPI_CS0n / FLASH_CS0n	/ GPIO1_D3_u	C23			FSPI_CS0n/FLASH_CS0n
	FSPI_D3 / FLASH_CS1n	/ GPIO1_D4_u	A27			FSPI_D3/FLASH_CS1n

Default is determined by Pin FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

VCCIO2 — H18

RK3568-Socket
BGA636_65Rx65Rx45R3_S





RK3568_J(VCCIO3 Domain)

U1000J

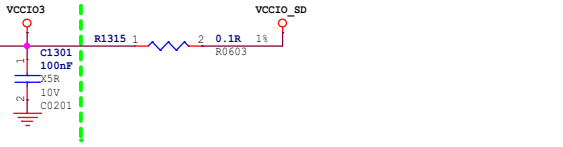
VCCIO3 Domain

Operating Voltage=1.8V/3.3V

SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/ PWM8_M1	/ GPIO1_D5_u	J25	SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1
SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/ PWM9_M1	/ GPIO1_D6_u	J24	SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1
SDMMC0_D2	/ ARMJTAG_TCK	/ UART5_CTSn_M0	/ GPIO1_D7_u	H26	SDMMC0_D2/ARMJTAG_TCK
SDMMC0_D3	/ ARMJTAG_TMS	/ UART5_RTSn_M0	/ GPIO2_A0_u	J23	SDMMC0_D3/ARMJTAG_TMS
SDMMC0_CMD	/ PWM10_M1	/ UART5_RX_M0 / CAN0_TX_M1	/ GPIO2_A1_u	H27	SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1
SDMMC0_CLK	/ TEST_CLKOUT	/ UART5_TX_M0 / CAN0_RX_M1	/ GPIO2_A2_d	H28	GPIO2_A2 R1313 22R SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0/CAN0_RX_M1

TP1302 TP_0.7

VCCIO3 — L22



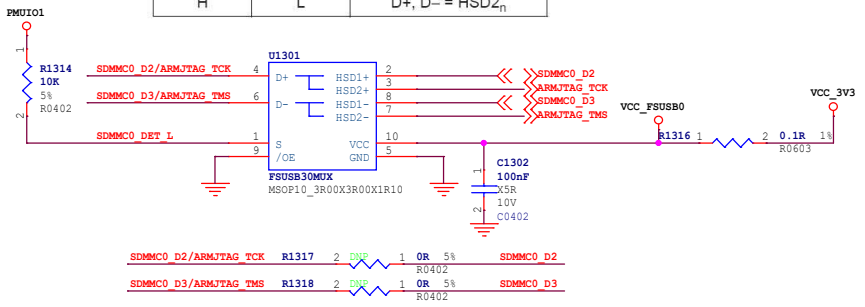
RK3568-Socket
BGA636_65Rx65Rx45R3_S

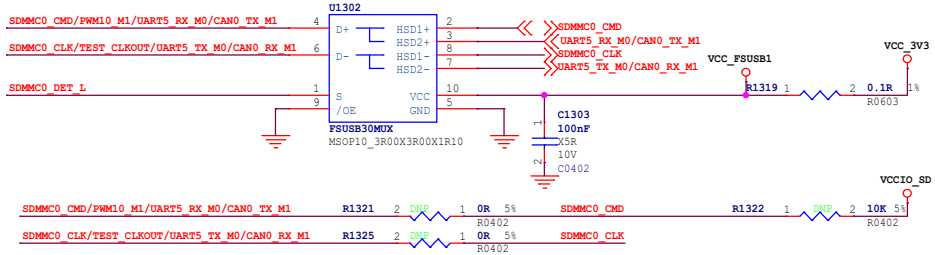
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

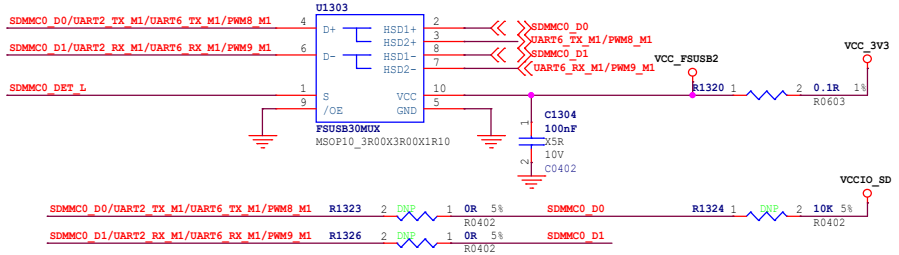
SDMMC0_DET_L

Truth Table

S	$\overline{OE}$	Function
X	H	Disconnect
L	L	D+, D– = $HSD1_n$
H	L	D+, D– = $HSD2_n$







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Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	13.RK3568_Flash/SD Controller				
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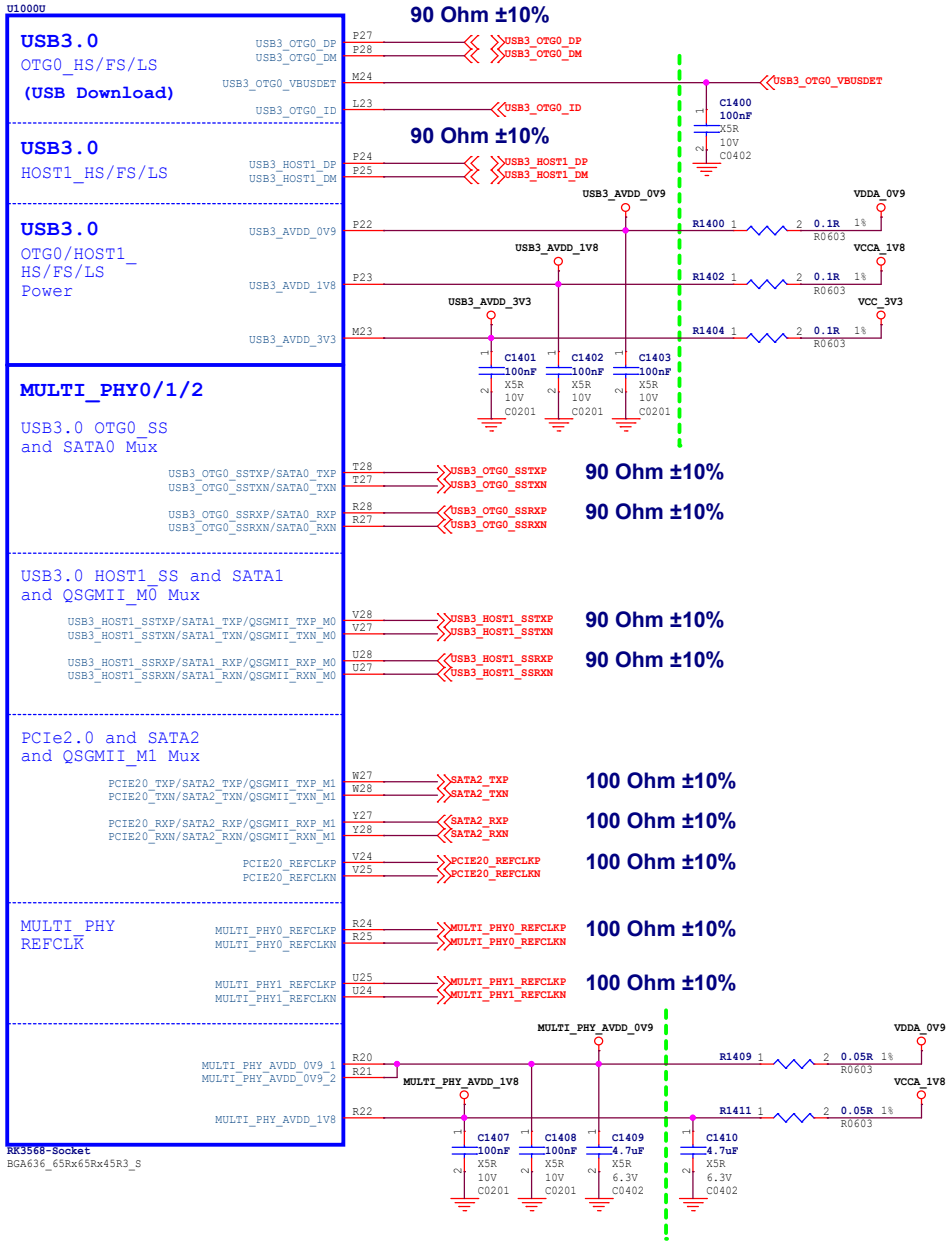
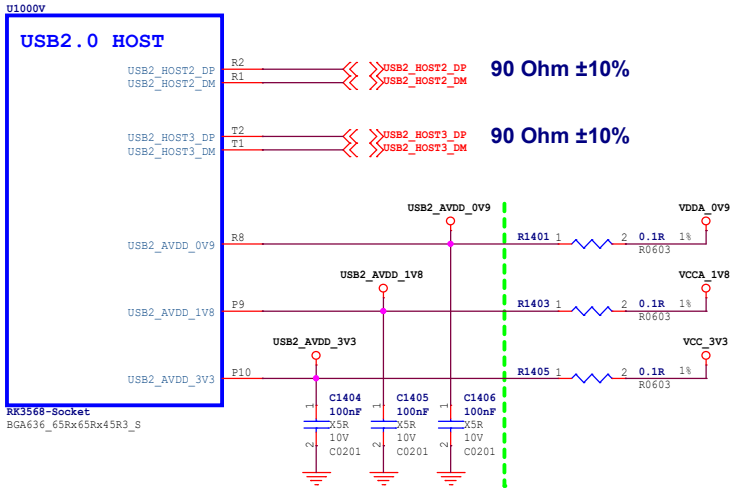
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



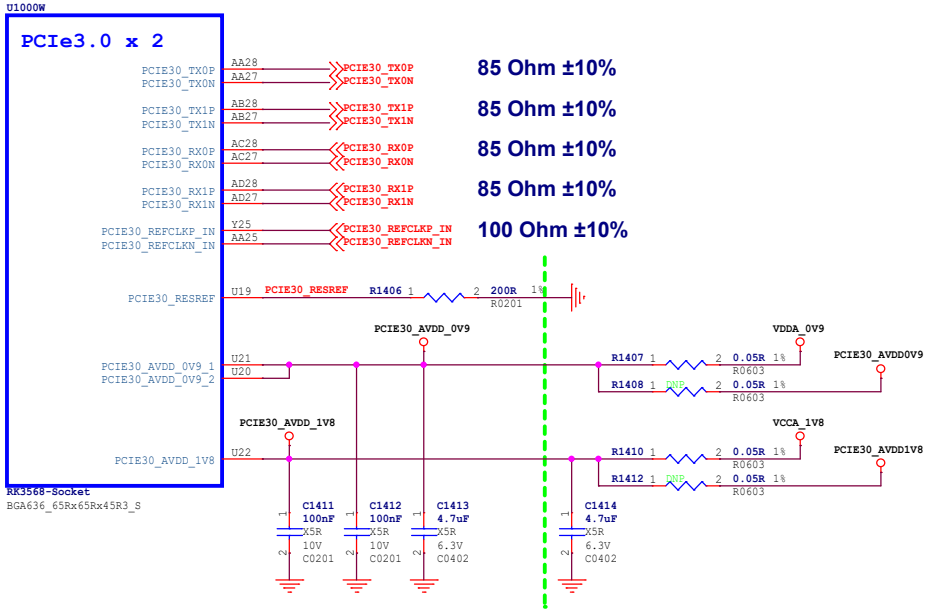
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_V(USB2.0 HOST)

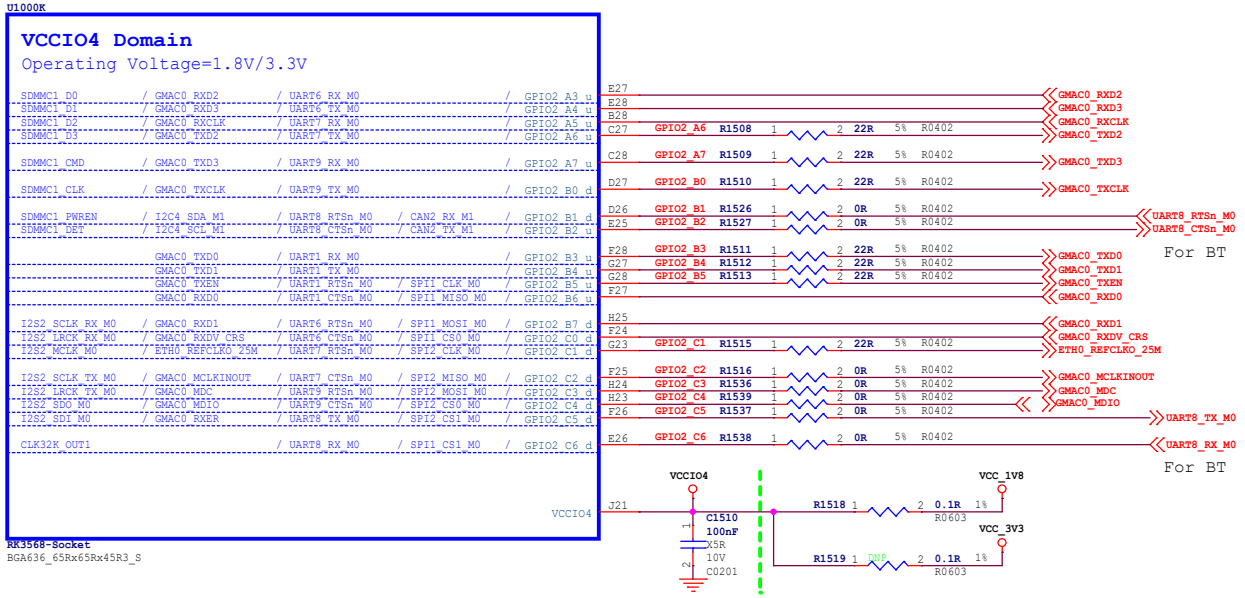


RK3568_W(PCIe3.0 x2)

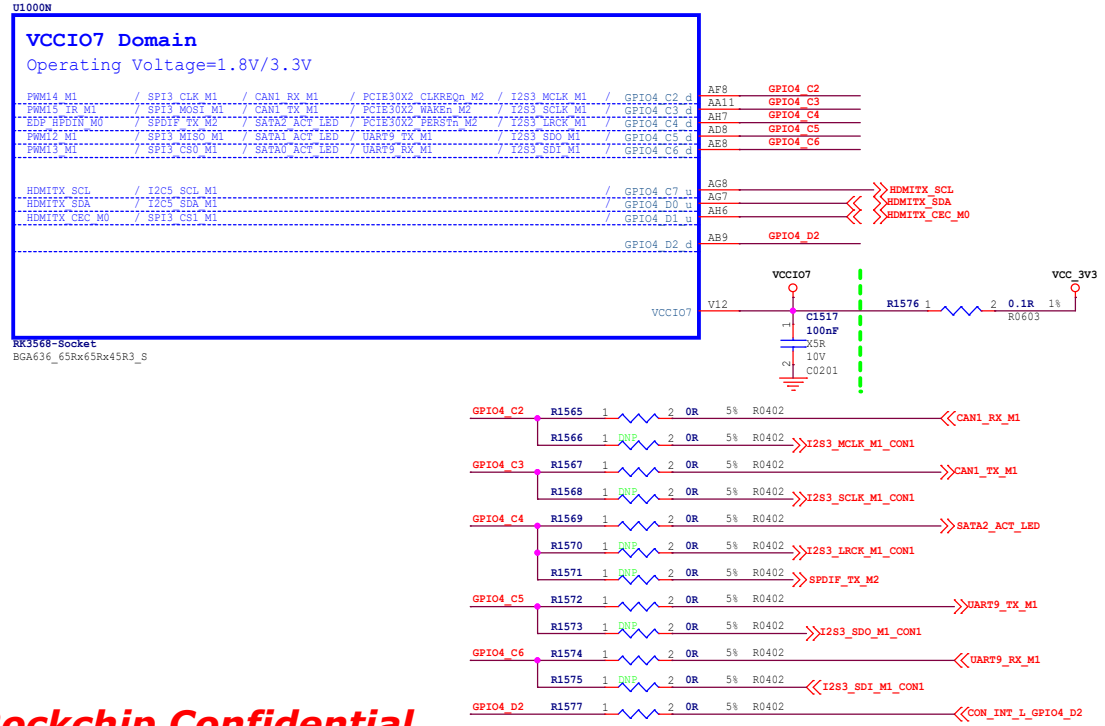


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	14.RK3568_USB/PCIe/SATA PHY				
Date:	Friday, September 25, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	14 of 50

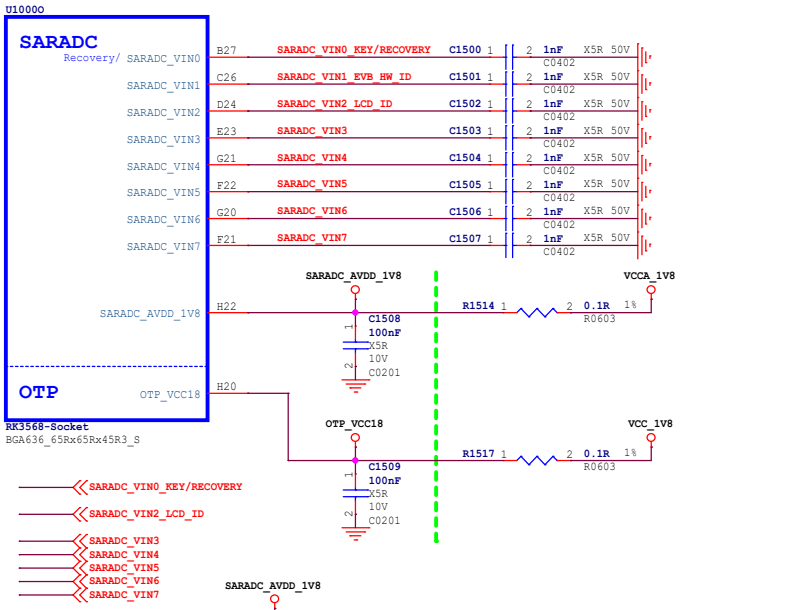
RK3568_K(VCCIO4 Domain)



RK3568_N(VCCIO7 Domain)

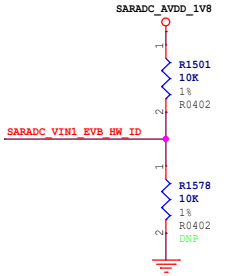


RK3568_O(SARADC/OTP)



Note:
Must be mounted

SARADC_VIN1_EVB_HW_ID	Rup	Rdown	ADC	
EVB1	10K	DNP	1023	1.8V
EVB2	20K	100K	852	1.5V
EVB3	18K	36K	681	1.2V
EVB4	51K	51K	512	0.9V
EVB5	36K	18K	340	0.6V
EVB6	100K	20K	170	0.3V
EVB7	DNP	10K	0	0V
EVB8				

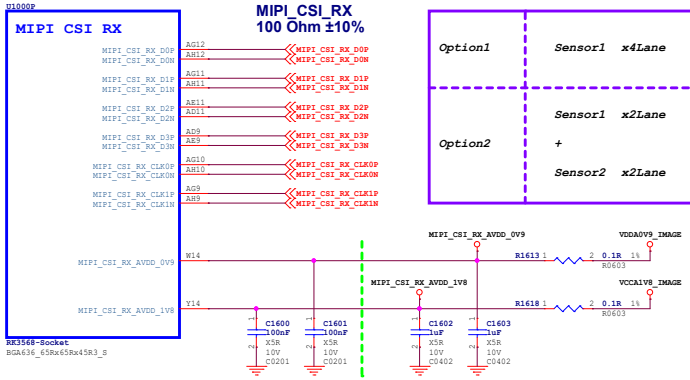


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

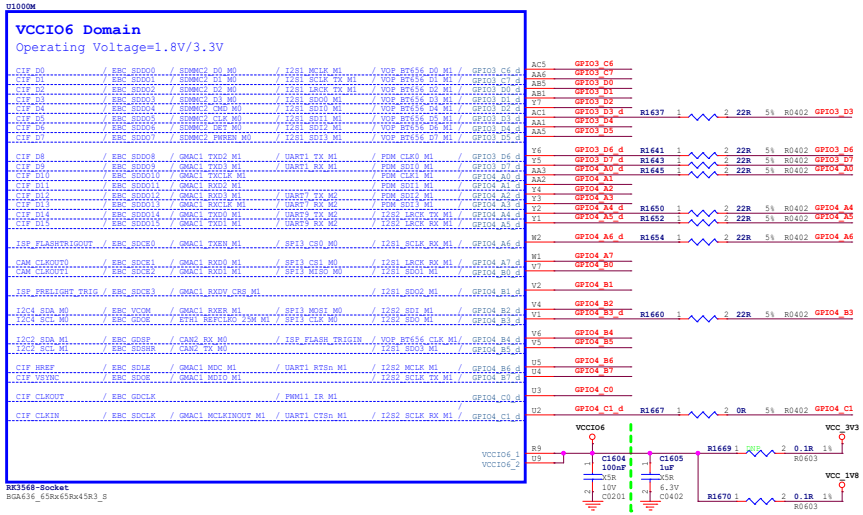
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3568_DDR4P216SD6		
File:	15.RK3568_SARADC/GPIO		
Date:	Wednesday, September 23, 2020	Rev:	V1.0
Designed by:	Zhangdz / Reviewed by: Default	Sheet:	15 of 50

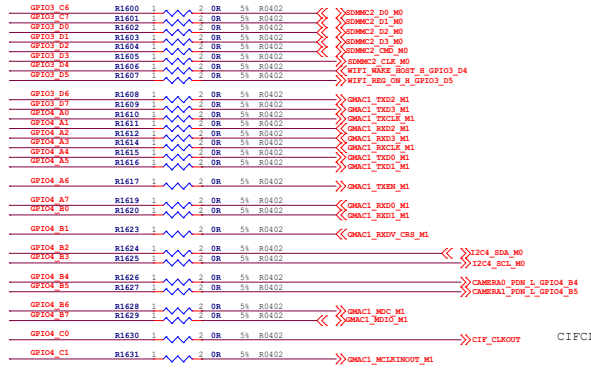
RK3568_P(MIPI_CSI_RX)

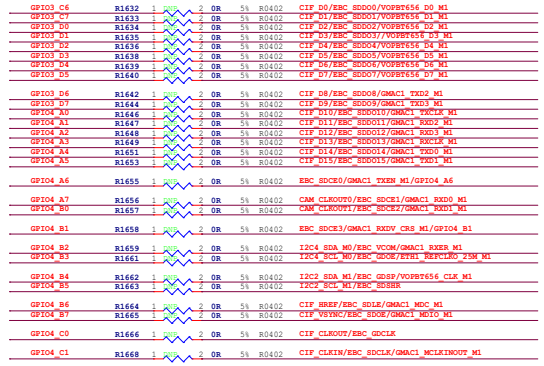


Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

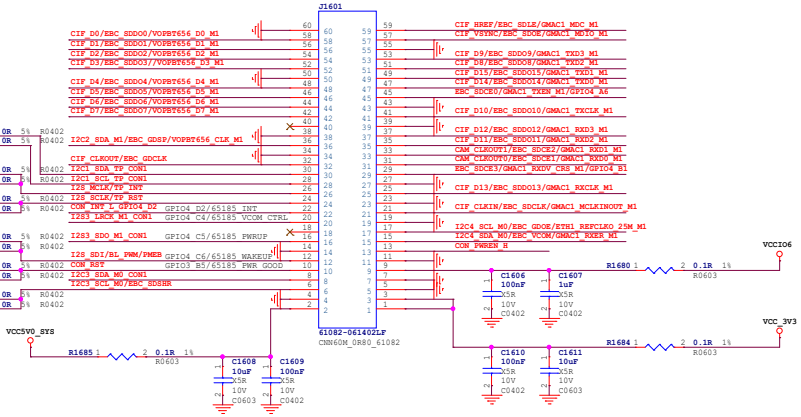
RK3568_M(VCCIO6 Domain)

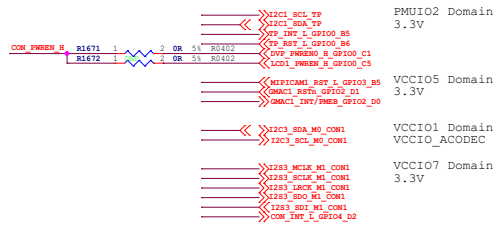






CIF,EBC,RGMII,BT656





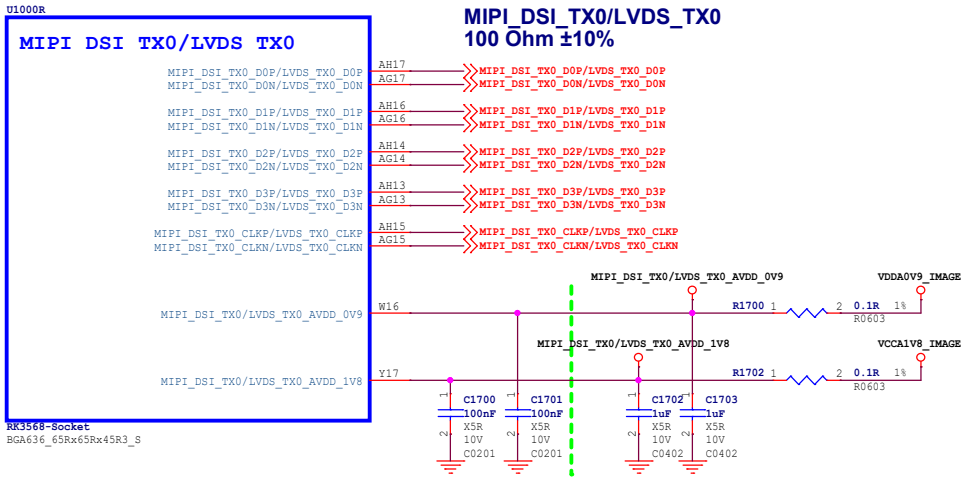
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

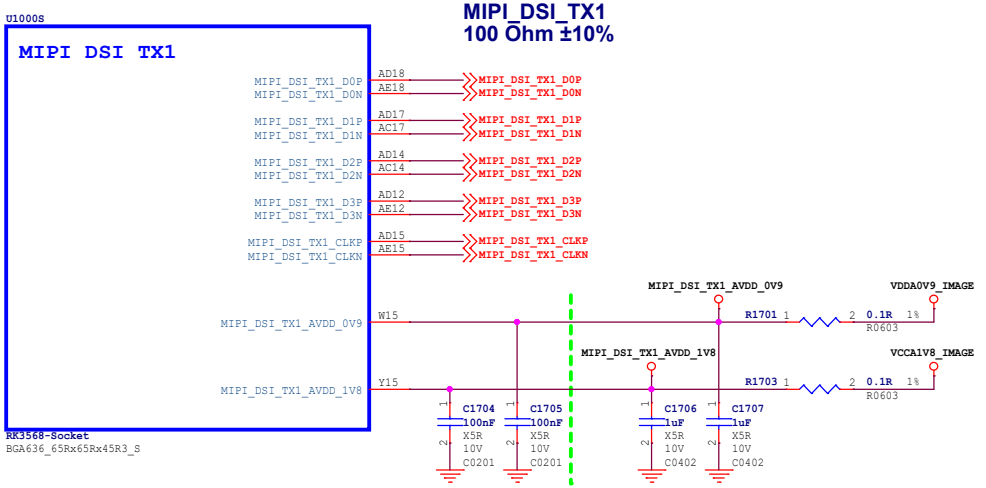
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3568_DDR4P216SD6		
File:	16.RK3568_VI Interface		
Date:	Wednesday, September 23, 2020	Rev:	V1.0
Designed by: Zhangtz	Reviewed by: Default	Sheet:	16 of 50

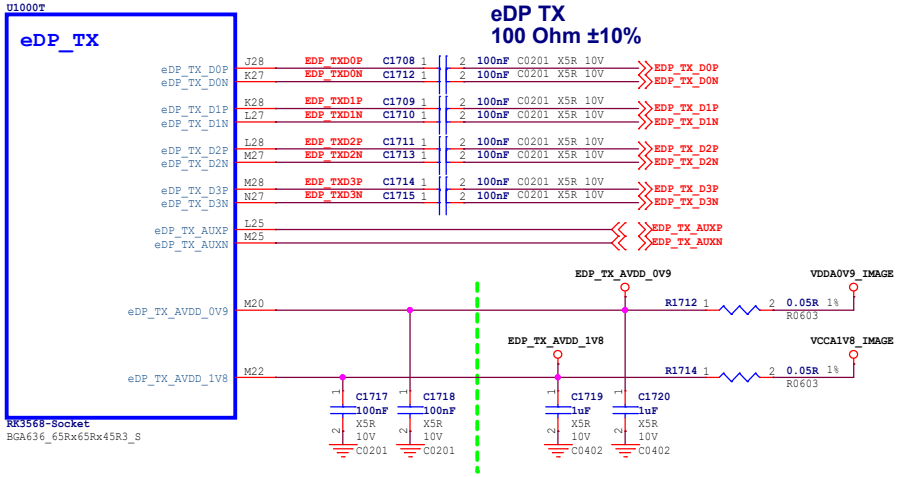
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



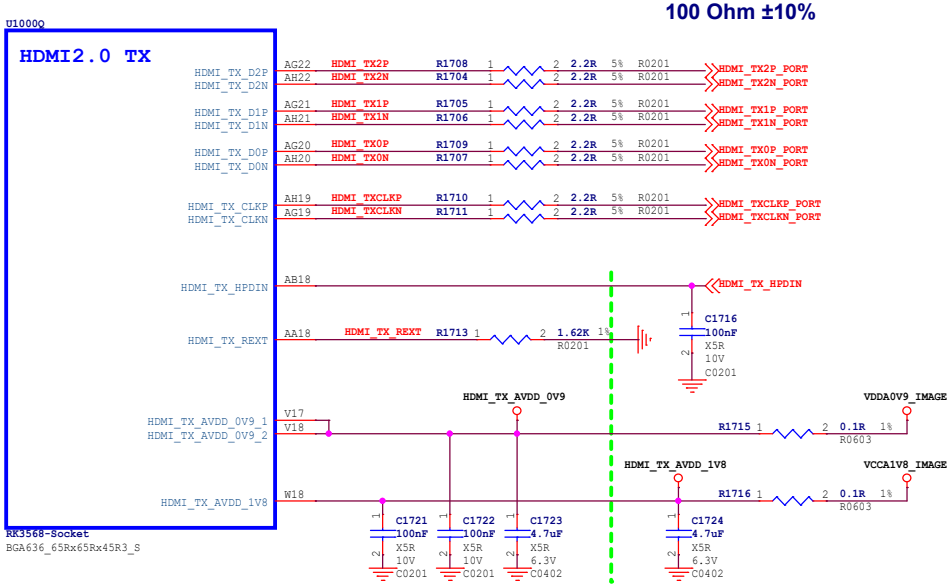
RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_Q(HDMI2.0 TX)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	17.RK3568_VO Interface_1				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	17 of 50

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	/ VOP_BT656_D0_M0	/ SPI0_MISO_M1	/ PCIE20_CLKREQn_M1	/ I2S1_MCLK_M2	/ GPIO2_D0_d
LCDC_D1	/ VOP_BT656_D1_M0	/ SPI0_MOSI_M1	/ PCIE20_WAKEn_M1	/ I2S1_SCLK_TX_M2	/ GPIO2_D1_d
LCDC_D2	/ VOP_BT656_D2_M0	/ SPI0_CS0_M1	/ PCIE30X1_CLKREQn_M1	/ I2S1_LRCK_TX_M2	/ GPIO2_D2_d
LCDC_D3	/ VOP_BT656_D3_M0	/ SPI0_CLK_M1	/ PCIE30X1_WAKEn_M1	/ I2S1_SDI0_M2	/ GPIO2_D3_d
LCDC_D4	/ VOP_BT656_D4_M0	/ SPI2_CS1_M1	/ PCIE30X2_CLKREQn_M1	/ I2S1_SDI1_M2	/ GPIO2_D4_d
LCDC_D5	/ VOP_BT656_D5_M0	/ SPI2_CS0_M1	/ PCIE30X2_WAKEn_M1	/ I2S1_SDI2_M2	/ GPIO2_D5_d
LCDC_D6	/ VOP_BT656_D6_M0	/ SPI2_MOSI_M1	/ PCIE30X2_PERSTn_M1	/ I2S1_SDI3_M2	/ GPIO2_D6_d
LCDC_D7	/ VOP_BT656_D7_M0	/ SPI2_MISO_M1	/ UART8_TX_M1	/ I2S1_SDO0_M2	/ GPIO2_D7_d
LCDC_CLK	/ VOP_BT656_CLK_M0	/ SPI2_CLK_M1	/ UART8_RX_M1	/ I2S1_SDO1_M2	/ GPIO3_A0_d
LCDC_D8	/ VOP_BT1120_D0	/ SPI1_CS0_M1	/ PCIE30X1_PERSTn_M1	/ SDMMC2_D0_M1	/ GPIO3_A1_d
LCDC_D9	/ VOP_BT1120_D1	/ GMAC1_TXD2_M0	/ I2S3_MCLK_M0	/ SDMMC2_D1_M1	/ GPIO3_A2_d
LCDC_D10	/ VOP_BT1120_D2	/ GMAC1_TXD3_M0	/ I2S3_SCLK_M0	/ SDMMC2_D2_M1	/ GPIO3_A3_d
LCDC_D11	/ VOP_BT1120_D3	/ GMAC1_RXD2_M0	/ I2S3_LRCK_M0	/ SDMMC2_D3_M1	/ GPIO3_A4_d
LCDC_D12	/ VOP_BT1120_D4	/ GMAC1_RXD3_M0	/ I2S3_SDO_M0	/ SDMMC2_CMD_M1	/ GPIO3_A5_d
LCDC_D13	/ VOP_BT1120_CLK	/ GMAC1_TXCLK_M0	/ I2S3_SDI_M0	/ SDMMC2_CLK_M1	/ GPIO3_A6_d
LCDC_D14	/ VOP_BT1120_D5	/ GMAC1_RXCLK_M0		/ SDMMC2_DET_M1	/ GPIO3_A7_d
LCDC_D15	/ VOP_BT1120_D6	/ ETH1_REFCLKO_25M_M0		/ SDMMC2_PWREN_M1	/ GPIO3_B0_d
LCDC_D16	/ VOP_BT1120_D7	/ GMAC1_RXD0_M0	/ UART4_RX_M1	/ PWM8_M0	/ GPIO3_B1_d
LCDC_D17	/ VOP_BT1120_D8	/ GMAC1_RXD1_M0	/ UART4_TX_M1	/ PWM9_M0	/ GPIO3_B2_d
LCDC_D18	/ VOP_BT1120_D9	/ GMAC1_RXDV_CRS_M0	/ I2C5_SCL_M0	/ PDM_SDI0_M2	/ GPIO3_B3_d
LCDC_D19	/ VOP_BT1120_D10	/ GMAC1_RXER_M0	/ I2C5_SDA_M0	/ PDM_SDI1_M2	/ GPIO3_B4_d
LCDC_D20	/ VOP_BT1120_D11	/ GMAC1_TXD0_M0	/ I2C3_SCL_M1	/ PWM10_M0	/ GPIO3_B5_d
LCDC_D21	/ VOP_BT1120_D12	/ GMAC1_TXD1_M0	/ I2C3_SDA_M1	/ PWM11_IR_M0	/ GPIO3_B6_d
LCDC_D22	/ PWM12_M0	/ GMAC1_TXEN_M0	/ UART3_TX_M1	/ PDM_SDI2_M2	/ GPIO3_B7_d
LCDC_D23	/ PWM13_M0	/ GMAC1_MCLKINOUT_M0	/ UART3_RX_M1	/ PDM_SDI3_M2	/ GPIO3_C0_d
LCDC_HSYNC	/ VOP_BT1120_D13	/ SPI1_MOSI_M1	/ PCIE20_PERSTn_M1	/ I2S1_SDO2_M2	/ GPIO3_C1_d
LCDC_VSYNC	/ VOP_BT1120_D14	/ SPI1_MISO_M1	/ UART5_TX_M1	/ I2S1_SDO3_M2	/ GPIO3_C2_d
LCDC_DEN	/ VOP_BT1120_D15	/ SPI1_CLK_M1	/ UART5_RX_M1	/ I2S1_SCLK_RX_M2	/ GPIO3_C3_d
PWM14_M0	/ VOP_PWM_M1	/ GMAC1_MDC_M0	/ UART7_TX_M1	/ PDM_CLK1_M2	/ GPIO3_C4_d
PWM15_IR_M0	/ SPDIF_TX_M1	/ GMAC1_MDIO_M0	/ UART7_RX_M1	/ I2S1_LRCK_RX_M2	/ GPIO3_C5_d

VCCIO5_1
VCCIO5_2

RK3568-Socket
BGA636_65Rx65Rx45R3_S

AG6 GMAC1_INT/PMEB_GPIO2_D0
AD7 GMAC1_RSTn_GPIO2_D1
AC8 GMAC0_INT/PMEB_GPIO2_D2
AC7 GMAC0_RSTn_GPIO2_D3
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 PCIE30X2_PRSNT_L_GPIO2_D7

VCCIO5
R1800 10K 5% R0402 1 2
R1801 10K 5% R0402 1 2
GMAC1_INT/PMEB_GPIO2_D0
GMAC0_INT/PMEB_GPIO2_D2
od

AH4 BT_REG_ON_H_GPIO3_A0
AB8 BT_WAKE_HOST_H_GPIO3_A1
AE5 HOST_WAKE_BT_H_GPIO3_A2
AG4 I2S3_SCLK_M0
AF4 I2S3_LRCK_M0
AH3 I2S3_SDO_M0
AG3 I2S3_SDI_M0
for BT

AH2 PCIECLKIC_OE_H_GPIO3_A7
AG2 ETH1_REFCLKO_25M_M0

VCCIO5
R1802 2.2K 5% R0402 1 2
R1803 2.2K 5% R0402 1 2
I2C5_SCL_M0
I2C5_SDA_M0

AG1 UART4_RX_M1
AF2 UART4_TX_M1
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 GPIO3_B5
AE3 GPIO3_B6
AD4 UART3_TX_M1
AD2 UART3_RX_M1

AD1 GSENSOR_INT_L_GPIO3_C1
AA7 HP_DET_L_GPIO3_C2
AC4 PA_EN_H_GPIO3_C3

AC3 PWM14_M0
AC2 SPDIF_TX_M1

VCCIO5
VCC_3V3
V10
V11
C1800 100nF X5R 10V C0201 1 2
C1801 1uF X5R 6.3V C0402 DNP 1 2
R1804 1 2 0.1R 1% R0603

GPIO3_B5
R1809 1 DNP 2 0R 5% R0402 LCD0_RST_L_GPIO3_B5
R1810 1 2 0R 5% R0402 MIPICAM1_RST_L_GPIO3_B5

GPIO3_B6
R1811 1 DNP 2 0R 5% R0402 LCD1_RST_L_GPIO3_B6
R1812 1 2 0R 5% R0402 MIPICAM0_RST_L_GPIO3_B6

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd			
Project:	RK_EVB1_RK3568_DDR4P216SD6			
File:	18.RK3568_VO Interface_2			
Date:	Wednesday, September 23, 2020		Rev:	V1.0
Designed by:	Zhangdz	Reviewed by: Default	Sheet:	18 of 50

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d
					VCCIO1

RK3568-Socket

BGA636_65Rx65Rx45R3_S

D18 I2C3_SDA
E18 I2C3_SCL

R1900 1 DNP 2 0R 5% R0402 — I2C3_SDA_M0_CON1
R1901 1 DNP 2 0R 5% R0402 — I2C3_SCL_M0_CON1
R1902 1 2 0R 5% R0402 — I2C3_SDA_M0
R1903 1 2 0R 5% R0402 — I2C3_SCL_M0

A19 I2S1_MCLK_M0

B19 I2S1_SCLK_TX_M0
F18 I2S1_SCLK_RX_M0/PDM_CLK1_M0

A20 I2S1_LRCK_TX_M0
C20 I2S1_LRCK_RX_M0/PDM_CLK0_M0

B20 I2S1_SDO0_M0
D20 I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0
E20 I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0
A21 I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0
B21 I2S1_SDI0_M0/PDM_SDI0_M0

VCCIO1 — H17 — R1904 1 — 2 0.1R 1% R0603 — VCCIO_ACODEC

C1900 100nF X5R 10V C0201

S1900 Dial_Switch_6 SW12_8R22X5R40X2R30

I2S1_MCLK_M0	1	12	I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0	2	11	I2S1_SCLK_TX_M0_RK809
I2S1_LRCK_TX_M0	3	10	I2S1_LRCK_TX_M0_RK809
I2S1_SDO0_M0	4	9	I2S1_SDO0_M0_RK809
I2S1_SDI0_M0/PDM_SDI0_M0	5	8	I2S1_SDI0_M0/PDM_SDI0_M0_RK809
I2S1_LRCK_RX_M0/PDM_CLK0_M0	6	7	PDM_CLK0_M0_RK809

Default:RK809+PDM MIC
S1900=ON
S1901=OFF

S1901 Dial_Switch_6 SW12_8R22X5R40X2R30

I2S1_MCLK_M0	12	1	I2S1_MCLK_M0_CON
I2S1_SCLK_TX_M0	11	2	I2S1_SCLK_TX_M0_CON
I2S1_LRCK_TX_M0	10	3	I2S1_LRCK_TX_M0_CON
I2S1_SDO0_M0	9	4	I2S1_SDO0_M0_CON
I2S1_SDI0_M0/PDM_SDI0_M0	8	5	I2S1_SDI0_M0/PDM_SDI0_M0_CON
I2S1_LRCK_RX_M0/PDM_CLK0_M0	7	6	I2S1_LRCK_RX_M0/PDM_CLK0_M0_CON

VCCIO1
R1905 2.2K 5% R0402
R1906 2.2K 5% R0402
I2C3_SDA_M0
I2C3_SCL_M0

I2S1_SCLK_RX_M0/PDM_CLK1_M0 — R1907 1 DNP 2 0R 5% R0402 — I2S1_SCLK_RX_M0/PDM_CLK1_M0_CON
R1908 1 DNP 2 0R 5% R0402 — SPDIF_TX_M0

I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0 — R1909 1 2 0R 5% R0402 — I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0_CON

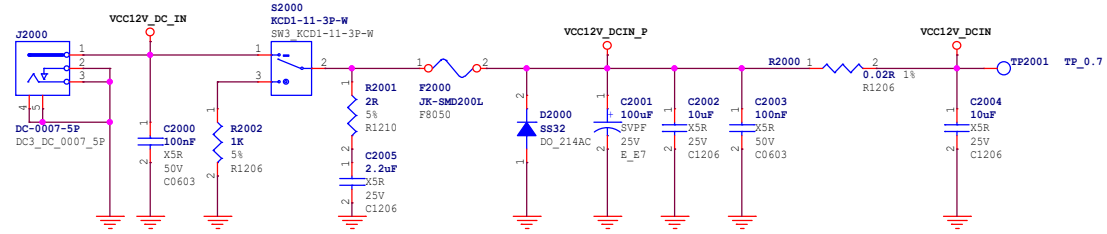
I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0 — R1910 1 2 0R 5% R0402 — I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0_CON

I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0 — R1911 1 2 0R 5% R0402 — I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0_CON

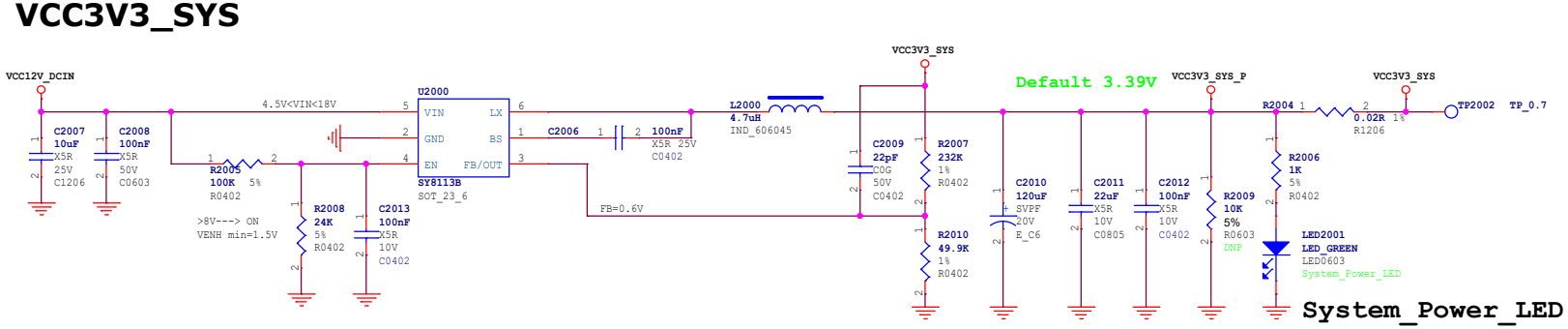
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	19.RK3568_Audio Interface				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	19 of 50

12V/3A DCIN

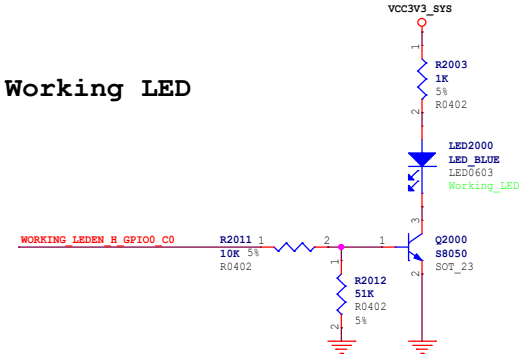


VCC3V3_SYS

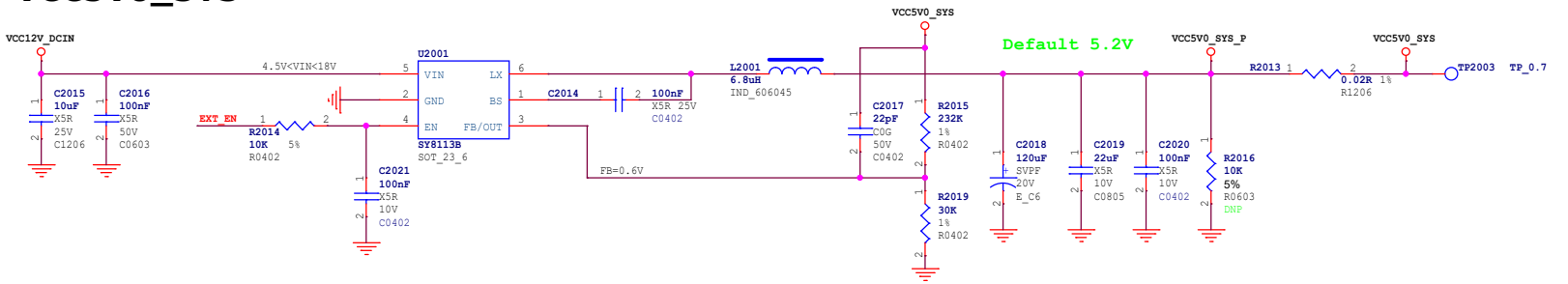


System_Power_LED

Working LED



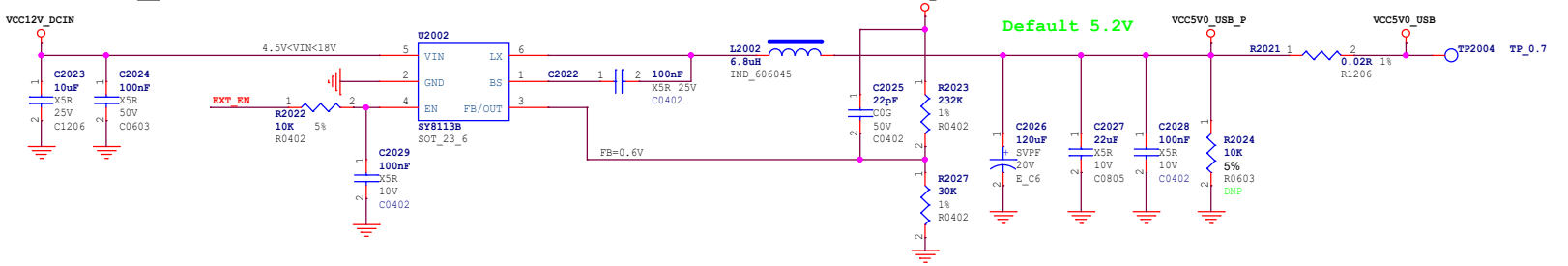
VCC5V0_SYS



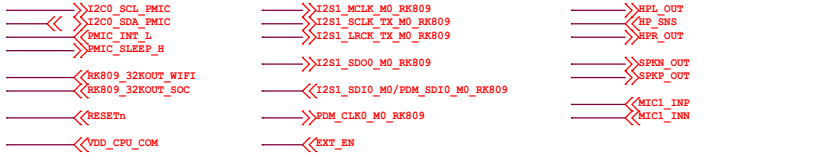
WORKING_LEDEN_H_GPIO0_C0

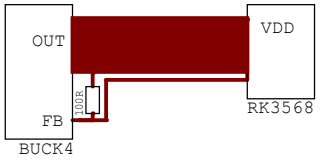
EXT_EN

VCC5V0_USB

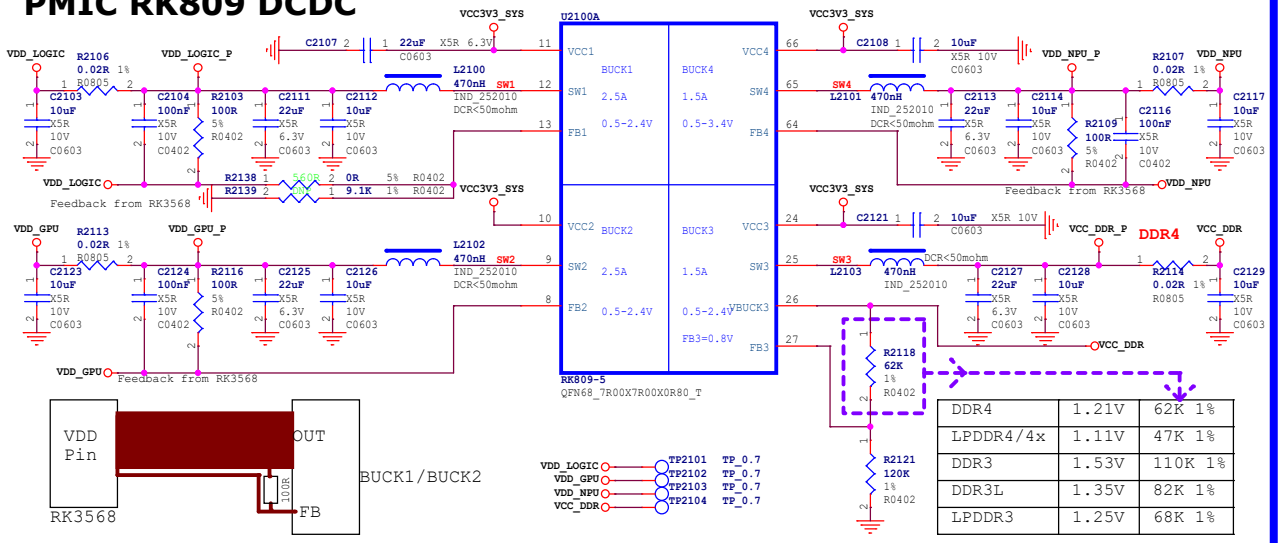


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	20.Power_DC IN				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	20 of 50



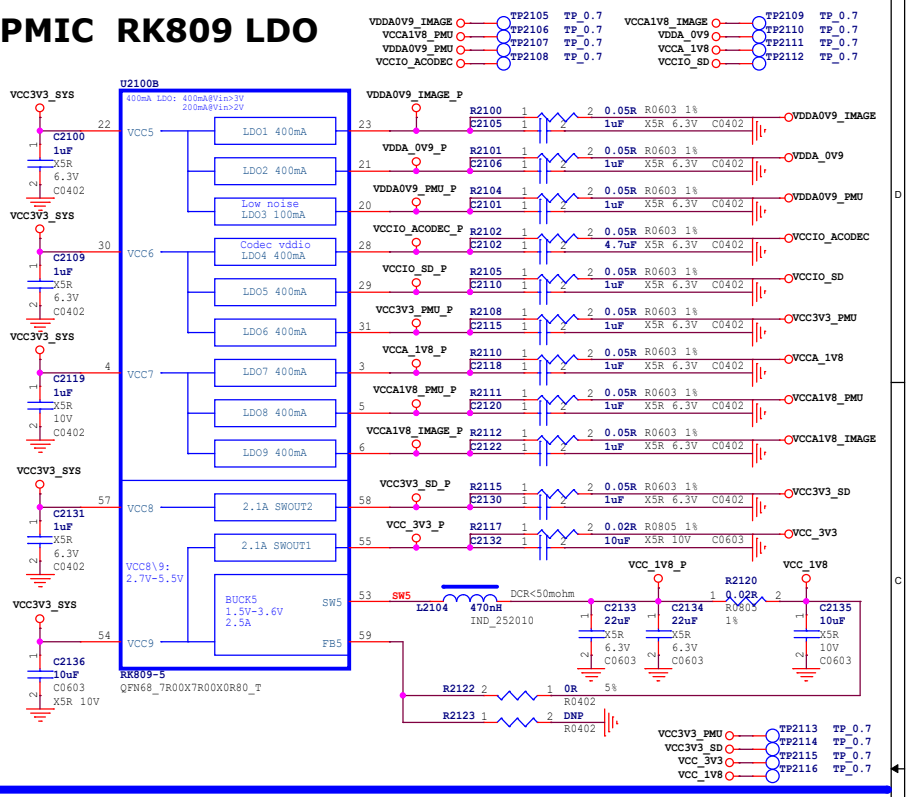


PMIC RK809 DCDC

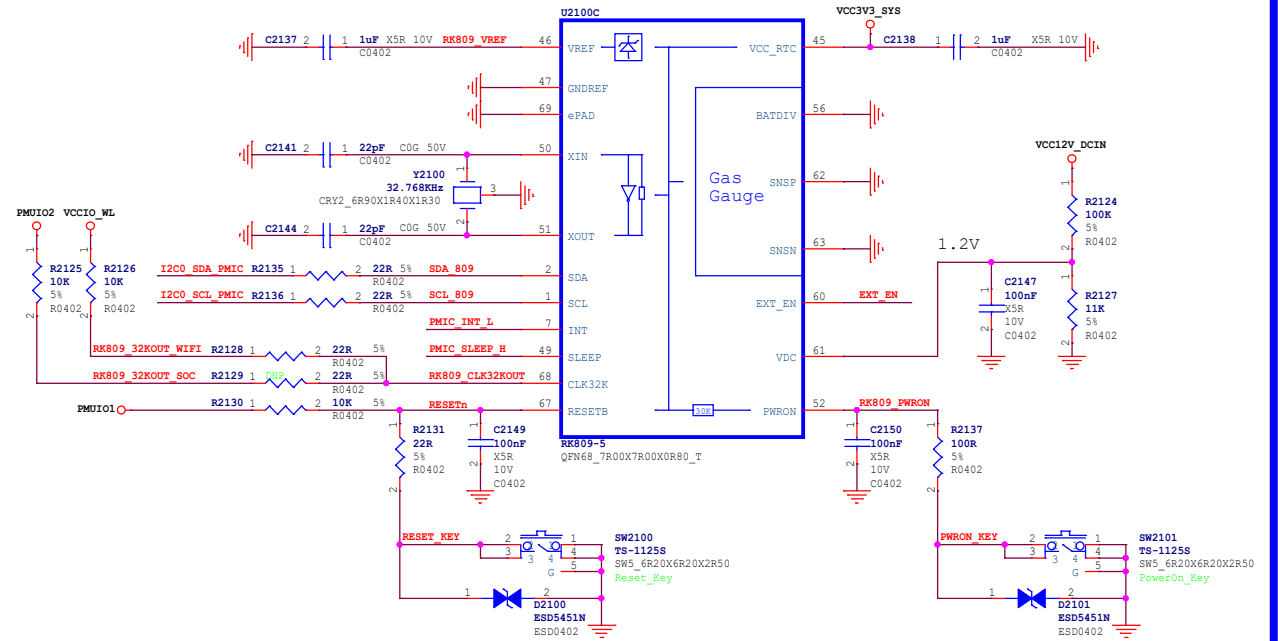


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

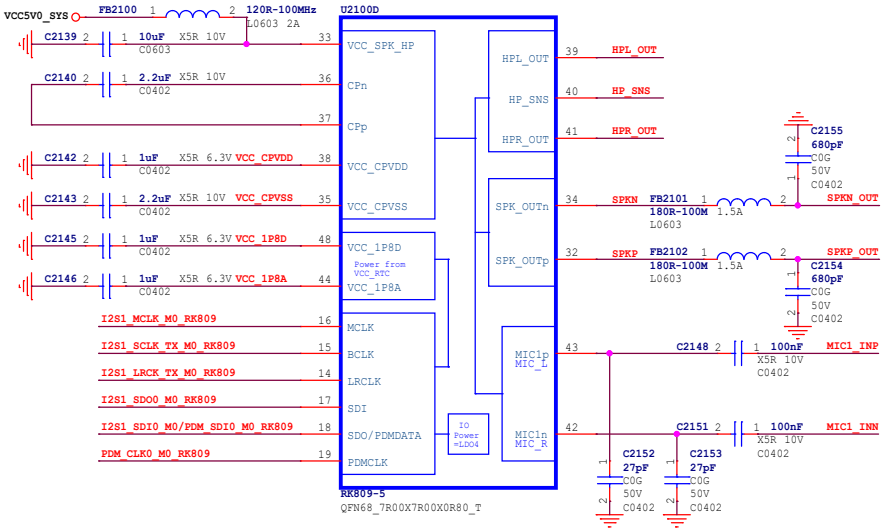
PMIC RK809 LDO



PMIC RK809 Managerment



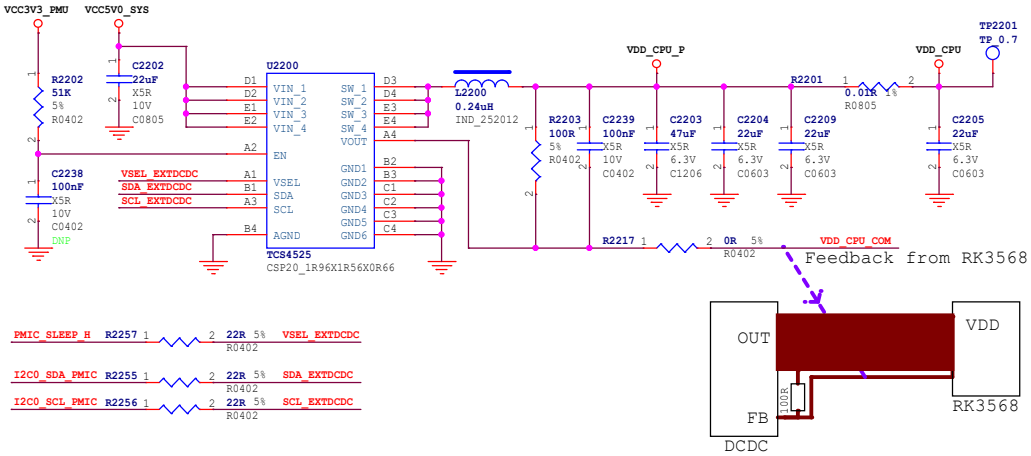
PMIC RK809 CODEC



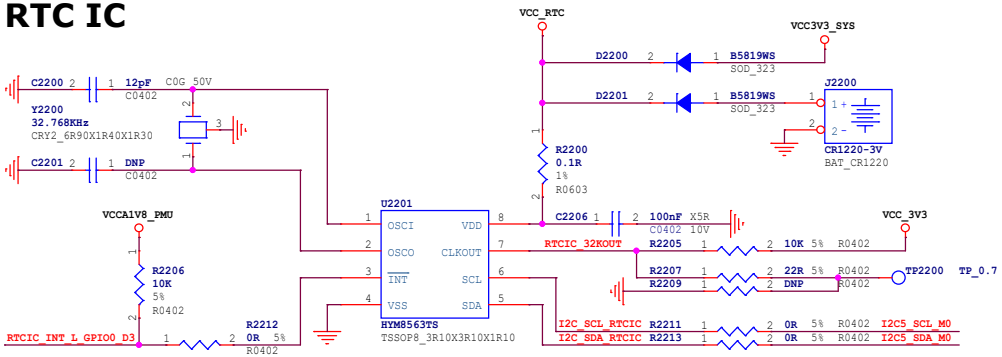
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	21.Power_PMIC				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	21 of 50

CPU_AVS/CPU_DVS_PWM0_M0
PMIC_SLEEP_H
VDD_CPU_COM
I2C0_SCL_PMIC
I2C0_SDA_PMIC
RTCIC_INT_L_GPIO0_D3
I2C5_SCL_M0
I2C5_SDA_M0

VDD_CPU

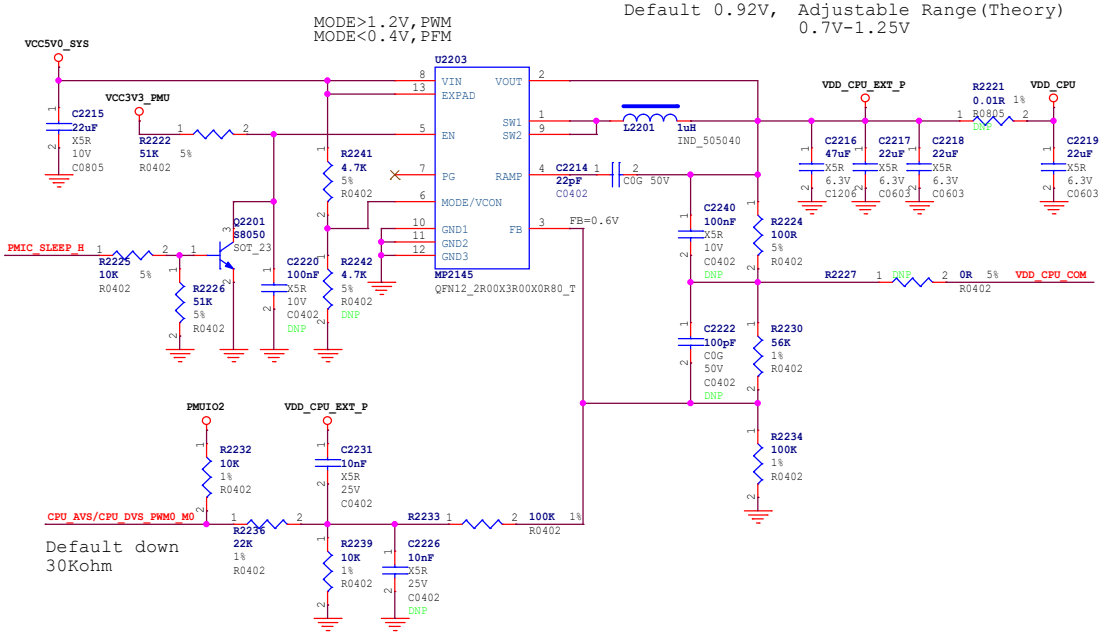


RTC IC

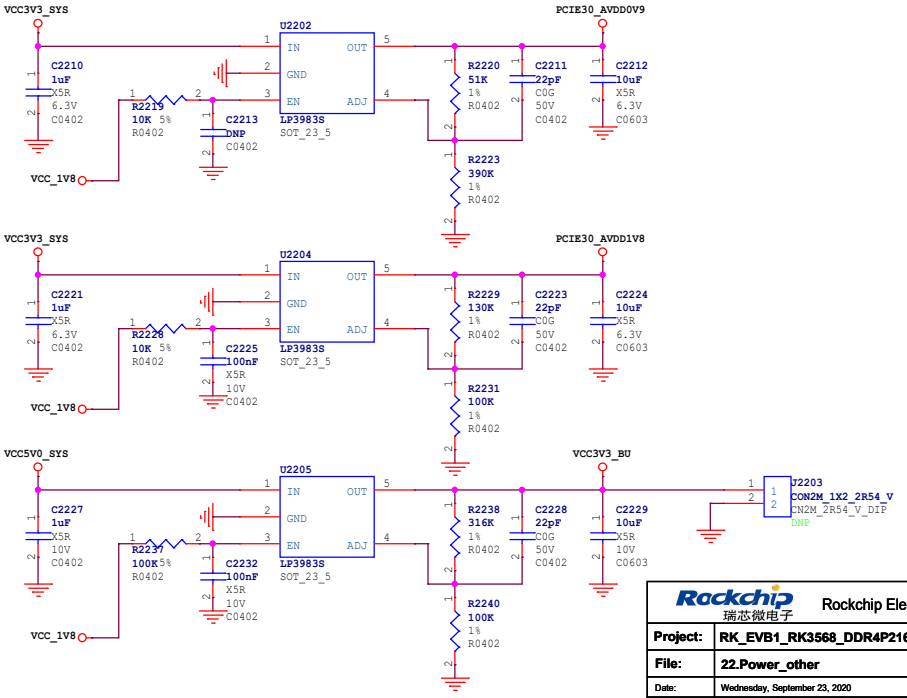


Address:Read A3H,Write A2H

VDD_CPU_EXT



Back-up Power



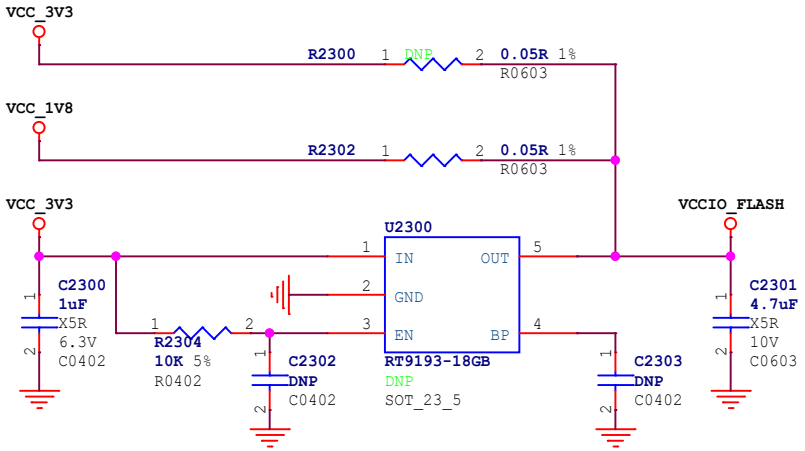
Rockchip Confidential

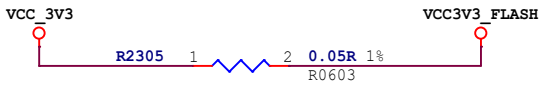
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	22.Power_other				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	22 of 50

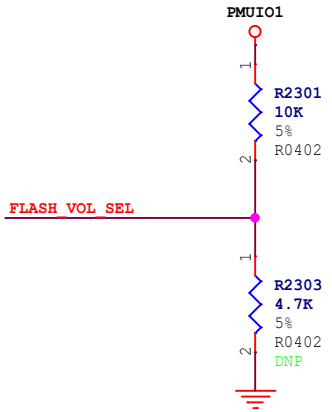
FLASH_VOL_SEL

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)

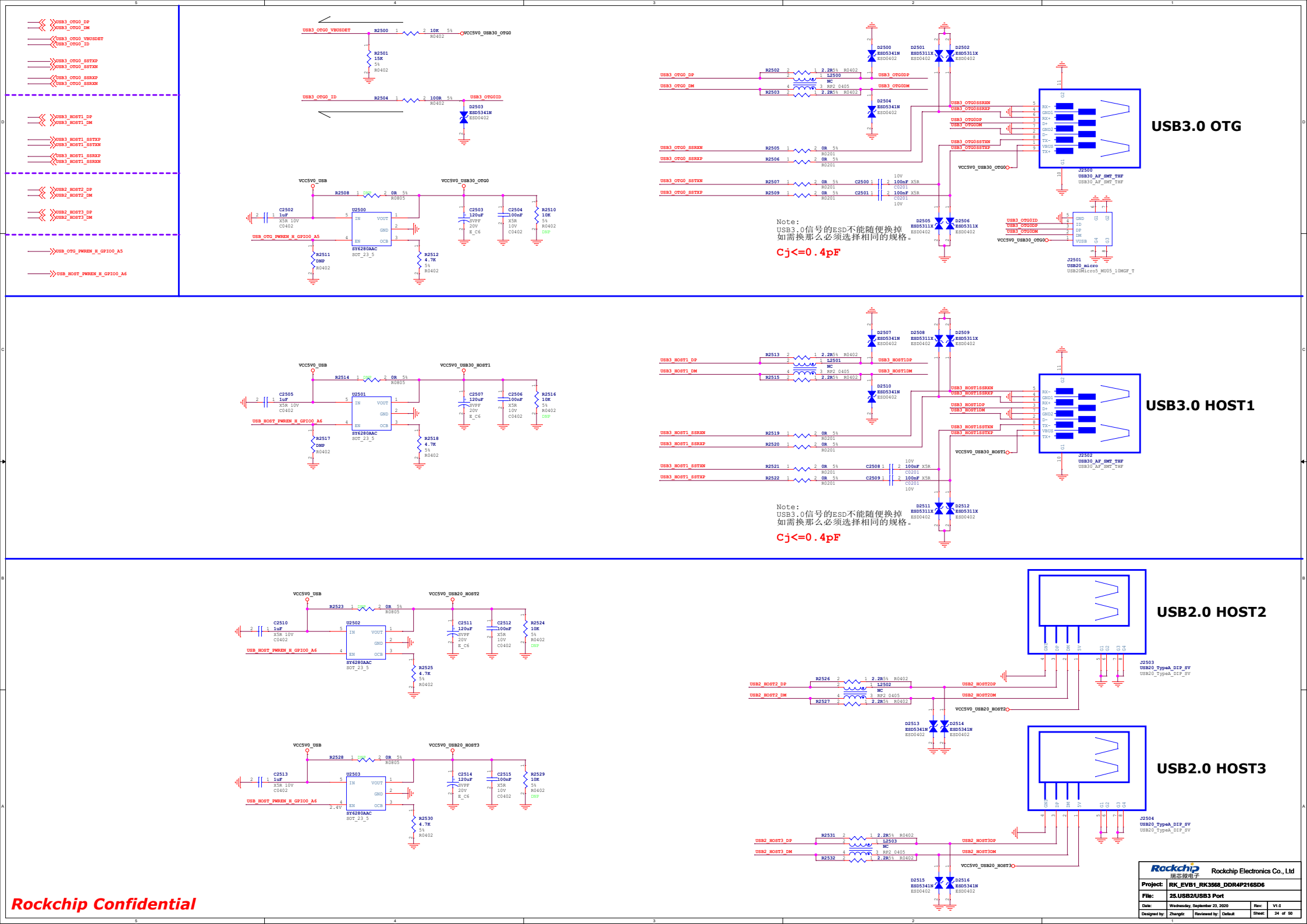




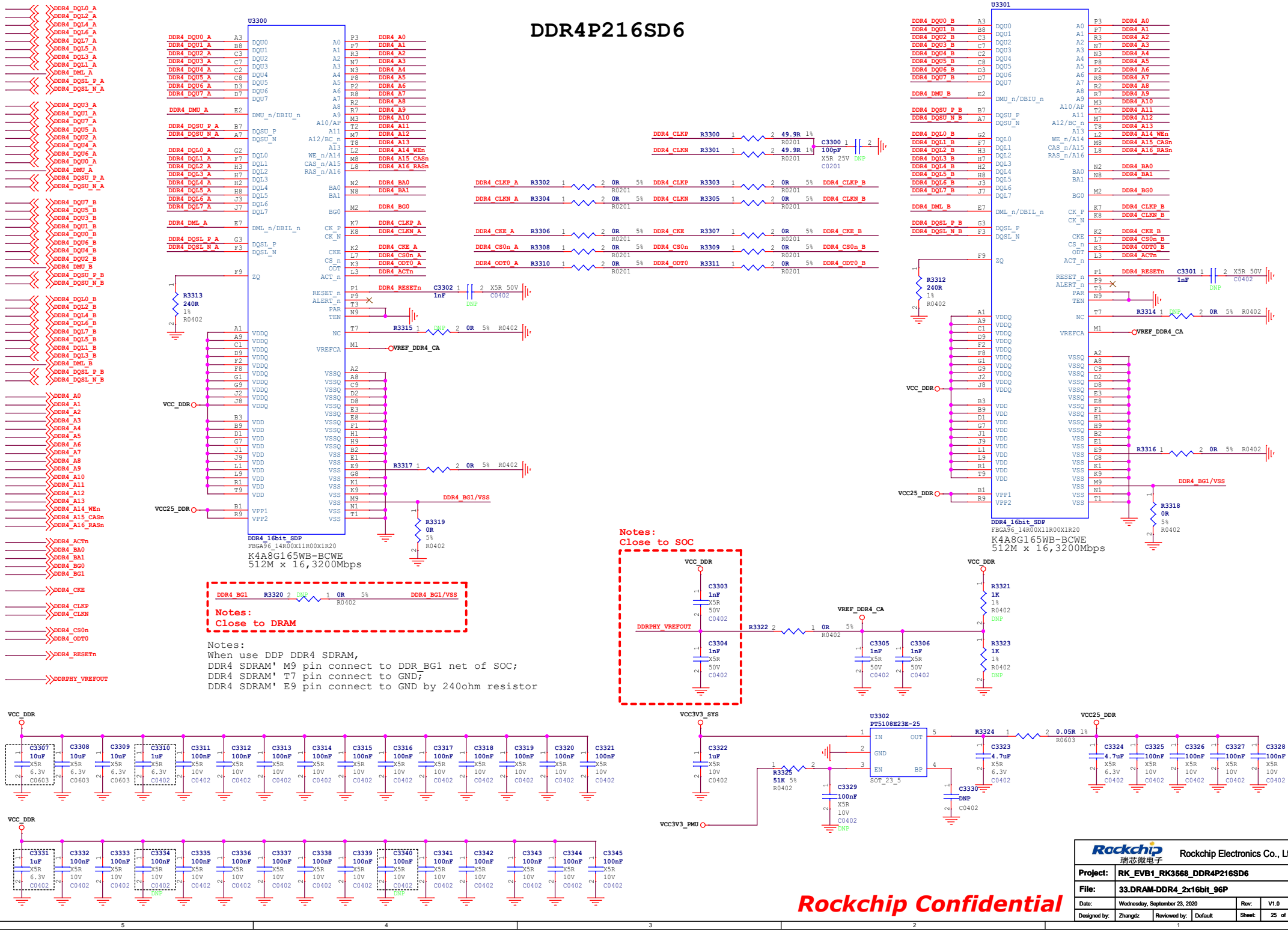


Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

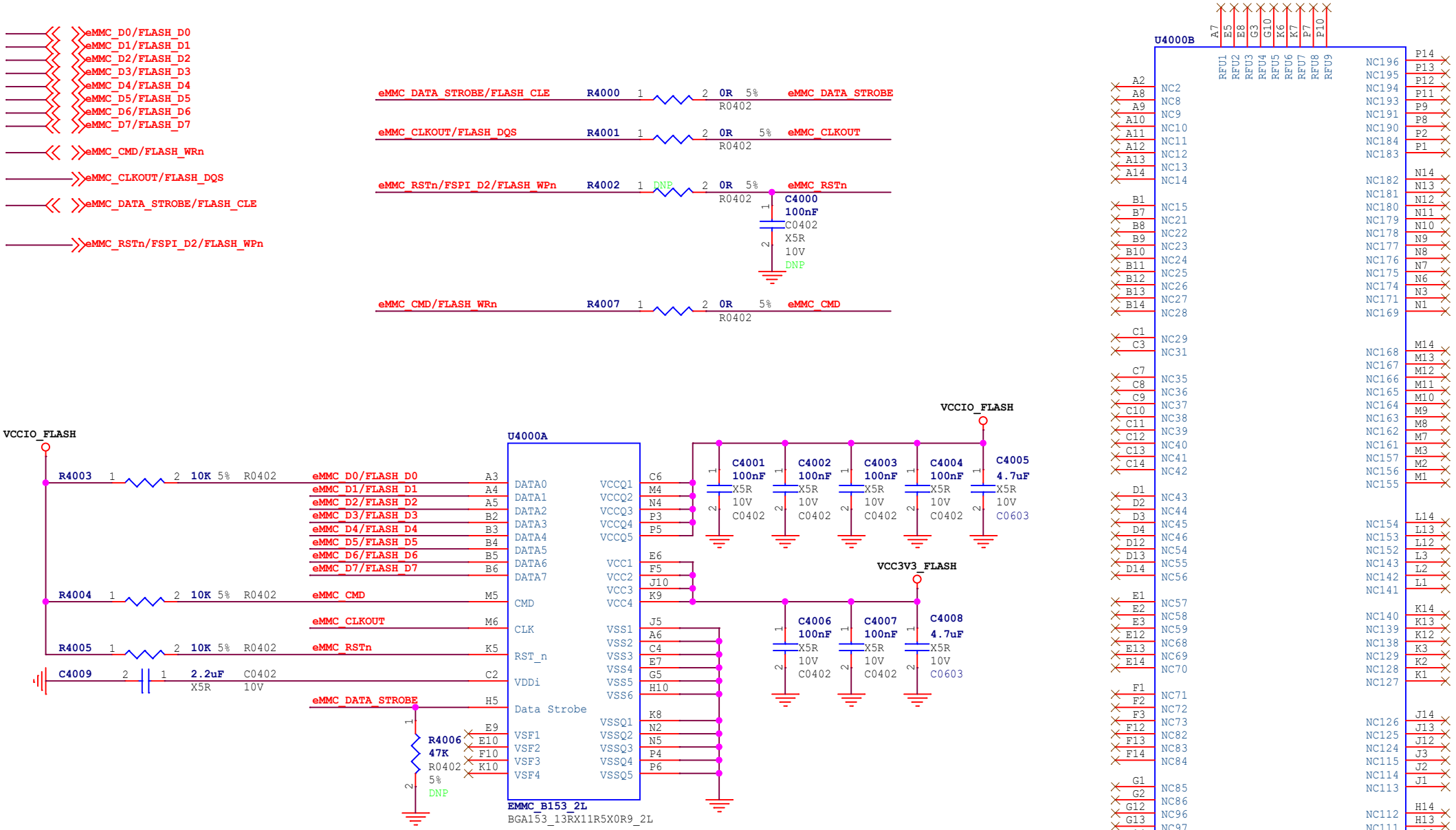
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	23.Power_Flash Power Manage				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	23 of 50


USB3.0 OTG
USB3.0 HOST1
USB2.0 HOST2
USB2.0 HOST3
Note:
USB3.0信号的ESD不能随便换掉
如需换那么必须选择相同的规格。
Cj<=0.4pF
Note:
USB3.0信号的ESD不能随便换掉
如需换那么必须选择相同的规格。
Cj<=0.4pF
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK_EVB1_RK3568_DDR4P216SD6
File: 25.USB2/USB3 Port
Date: Wednesday, September 23, 2020
Rev: V1.0
Designed by: Zhangtz
Reviewed by: Default
Sheet: 24 of 50

DDR4P216SD6



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3568_DDR4P216SD6		
File:	33.DRAM-DDR4_2x16bit_96P		
Date:	Wednesday, September 23, 2020	Rev:	V1.0
Designed by:	Zhangdz	Reviewed by: Default	Sheet: 25 of 50

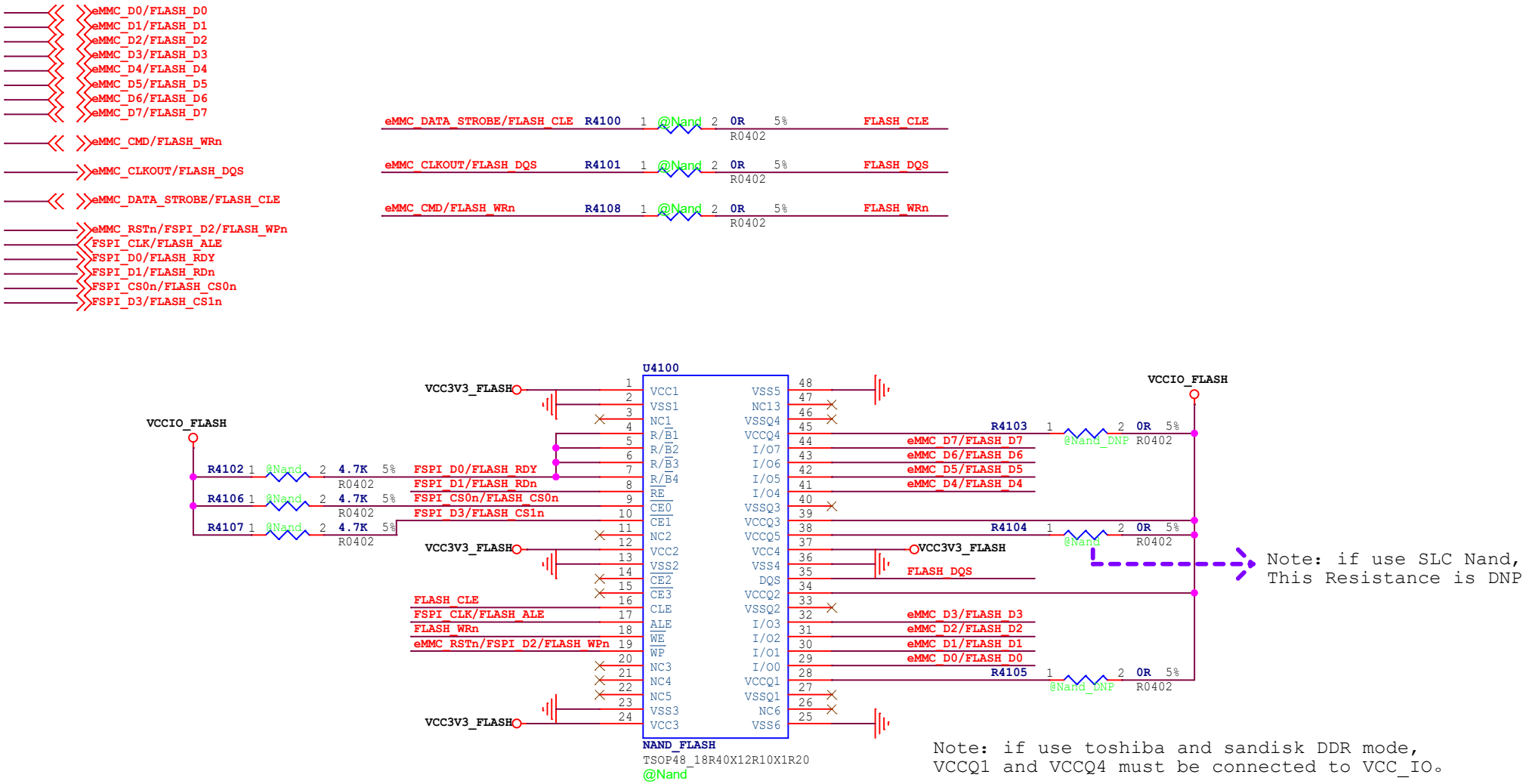


KLMBG2JETD-B041

SDINBDA6-32G-XI1

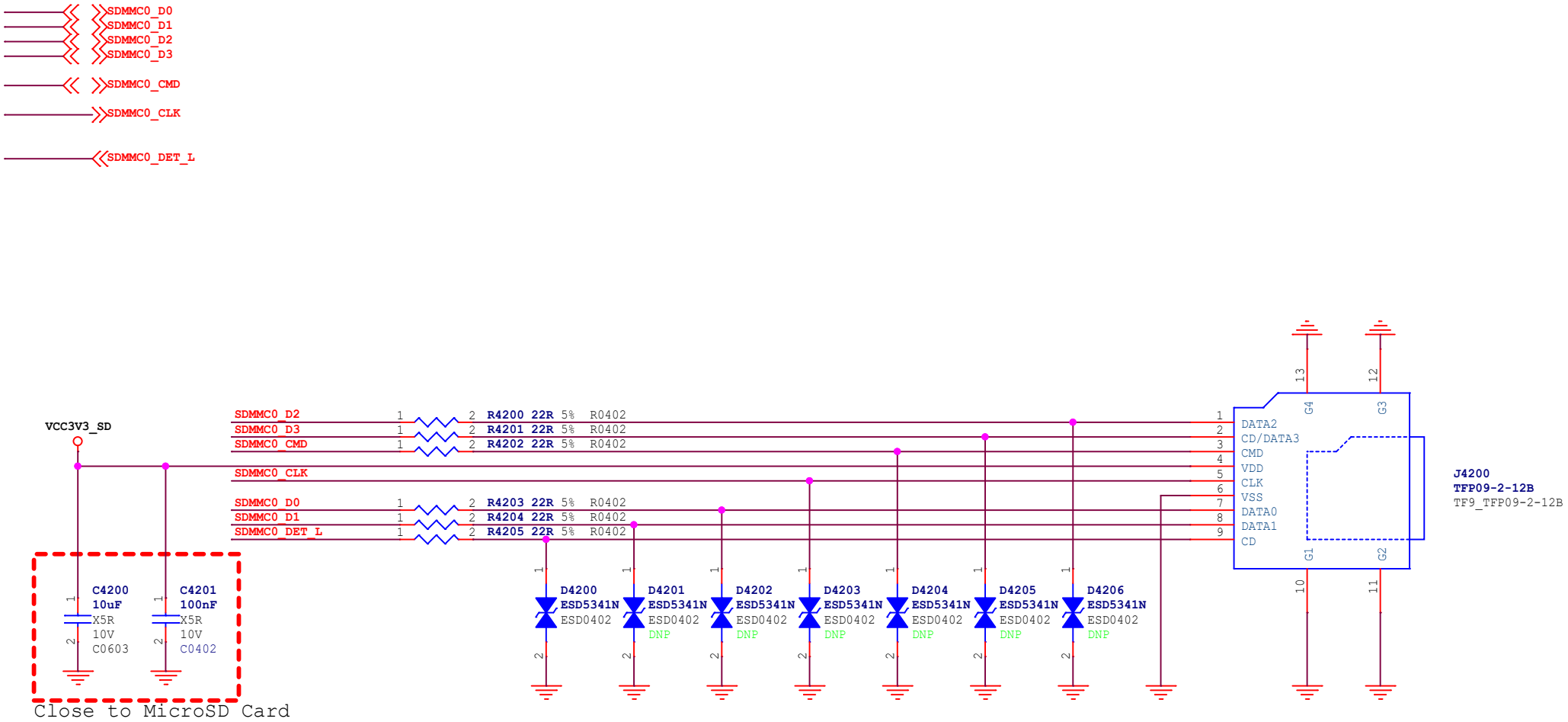
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	40.Flash-eMMC Flash				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	26 of 50



Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	41.Flash-Nand Flash(Option)				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	27 of 50



MicroSD Card

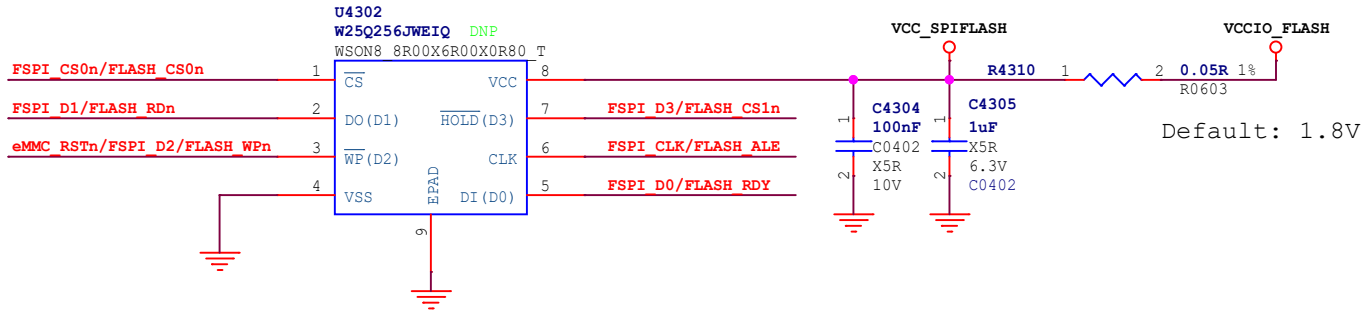
Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	42.Flash-MicroSD Card				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	28 of 50

FSPI_CLK/FLASH_ALE

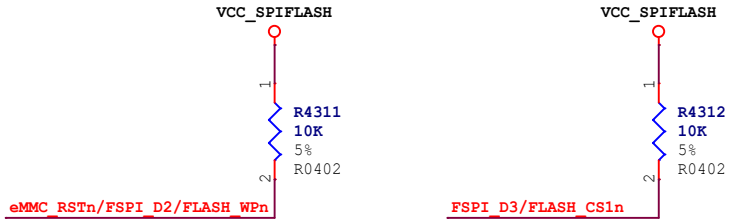
FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_D3/FLASH_CS1n

FSPI_CS0n/FLASH_CS0n



SPI Nor: W25Q256JWEIQ 1.8V

W25Q256FV, GD25Q256D 3.3V

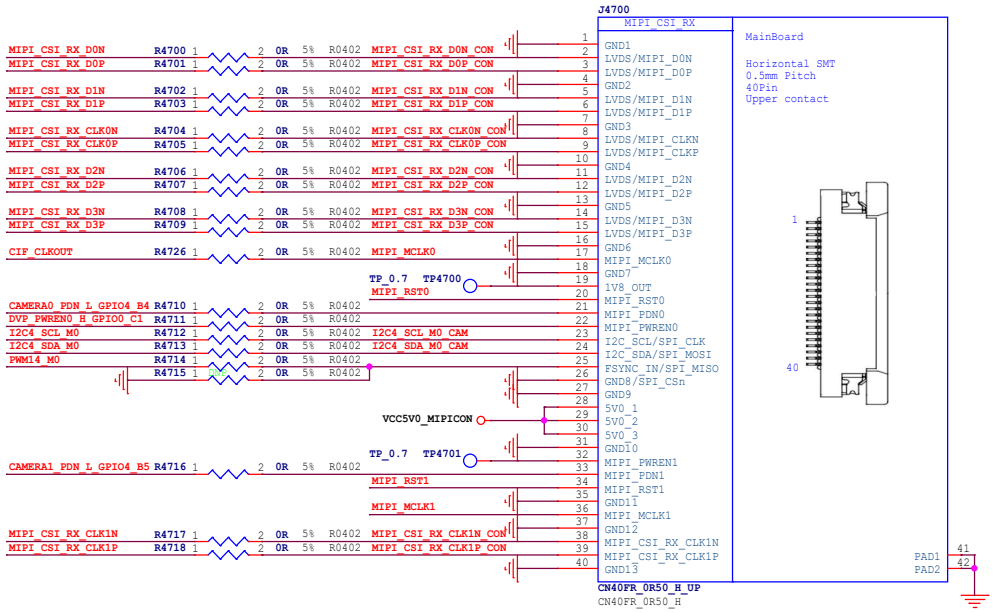


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	43.Flash-SPI FLASH				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	29 of 50

MIPI-CSI_RX CON

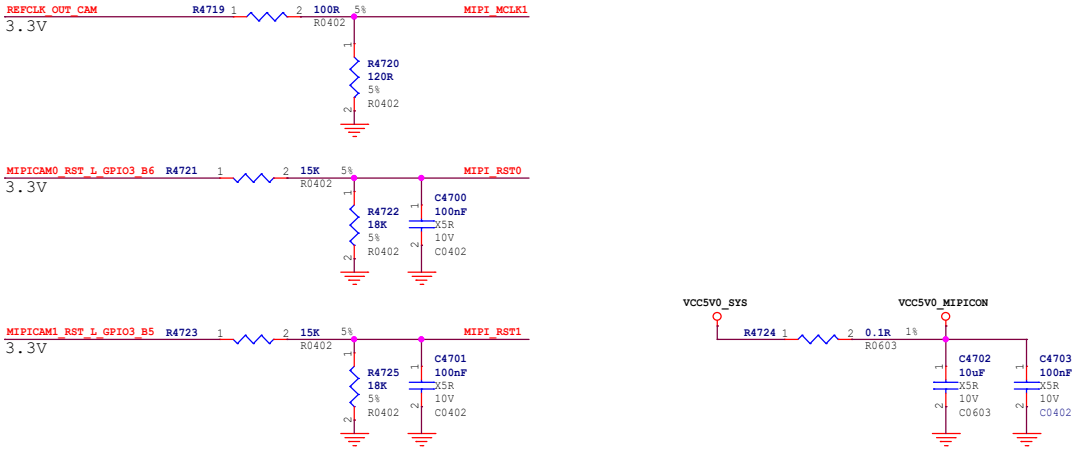
MIPI_CSI_RX_D0P
MIPI_CSI_RX_D0N
MIPI_CSI_RX_D1P
MIPI_CSI_RX_D1N
MIPI_CSI_RX_D2P
MIPI_CSI_RX_D2N
MIPI_CSI_RX_D3P
MIPI_CSI_RX_D3N
MIPI_CSI_RX_CLK0P
MIPI_CSI_RX_CLK0N
MIPI_CSI_RX_CLK1P
MIPI_CSI_RX_CLK1N
CIF_CLKOUT
REFCLK_OUT_CAM
I2C4_SDA_M0
I2C4_SCL_M0
CAMERA0_PDN_L_GPIO4_B4
CAMERA1_PDN_L_GPIO4_B5
MIPICAM1_RST_L_GPIO3_B5
MIPICAM0_RST_L_GPIO3_B6
DVP_PWREN0_H_GPIO0_C1
PWM14_M0

VCCIO5 Domain
3.3V

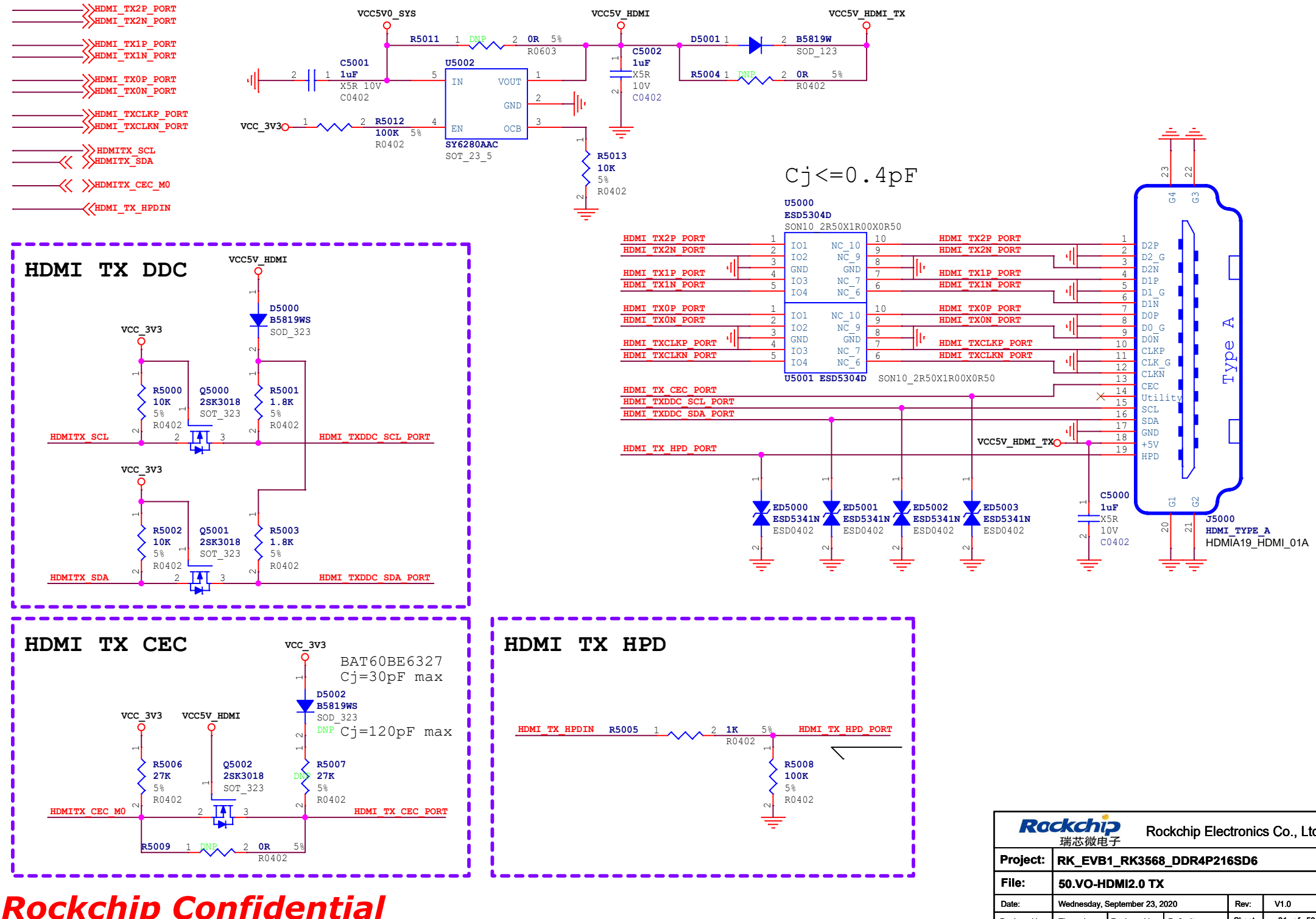


FPC Pin List

Pin1 :GND	
Pin2 :D0N	
Pin3 :D0P	
Pin4 :GND	
Pin5 :D1N	
Pin6 :D1P	
Pin7 :GND	
Pin8 :CLK0N	
Pin9 :CLK0P	
Pin10:GND	
Pin11:D2N	
Pin12:D2P	
Pin13:GND	
Pin14:D3N	
Pin15:D3P	
Pin16:GND	
Pin17:MIPI_MCLK0	1.8V
Pin18:GND	
Pin19:1V8_OUT	
Pin20:MIPI_RST0	1.8V
Pin21:MIPI_PDN0	1.8V
Pin22:MIPI_PWREN0	1.8V-3.3V
Pin23:I2C_SCL	1.8V
Pin24:I2C_SDA	1.8V
Pin25:GND/FSYNC_IN	1.8V
Pin26:GND	
Pin27:GND	
Pin28:5V0_IN	
Pin29:5V0_IN	
Pin30:5V0_IN	
Pin31:GND	
Pin32:MIPI_PWREN1	1.8V-3.3V
Pin33:MIPI_PDN1	1.8V
Pin34:MIPI_RST1	1.8V
Pin35:GND	
Pin36:MIPI_MCLK1	1.8V
Pin37:GND	
Pin38:CLK1N	
Pin39:CLK1P	
Pin40:GND	



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	47.VI-Camera_MIPI-CSI				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	30 of 50



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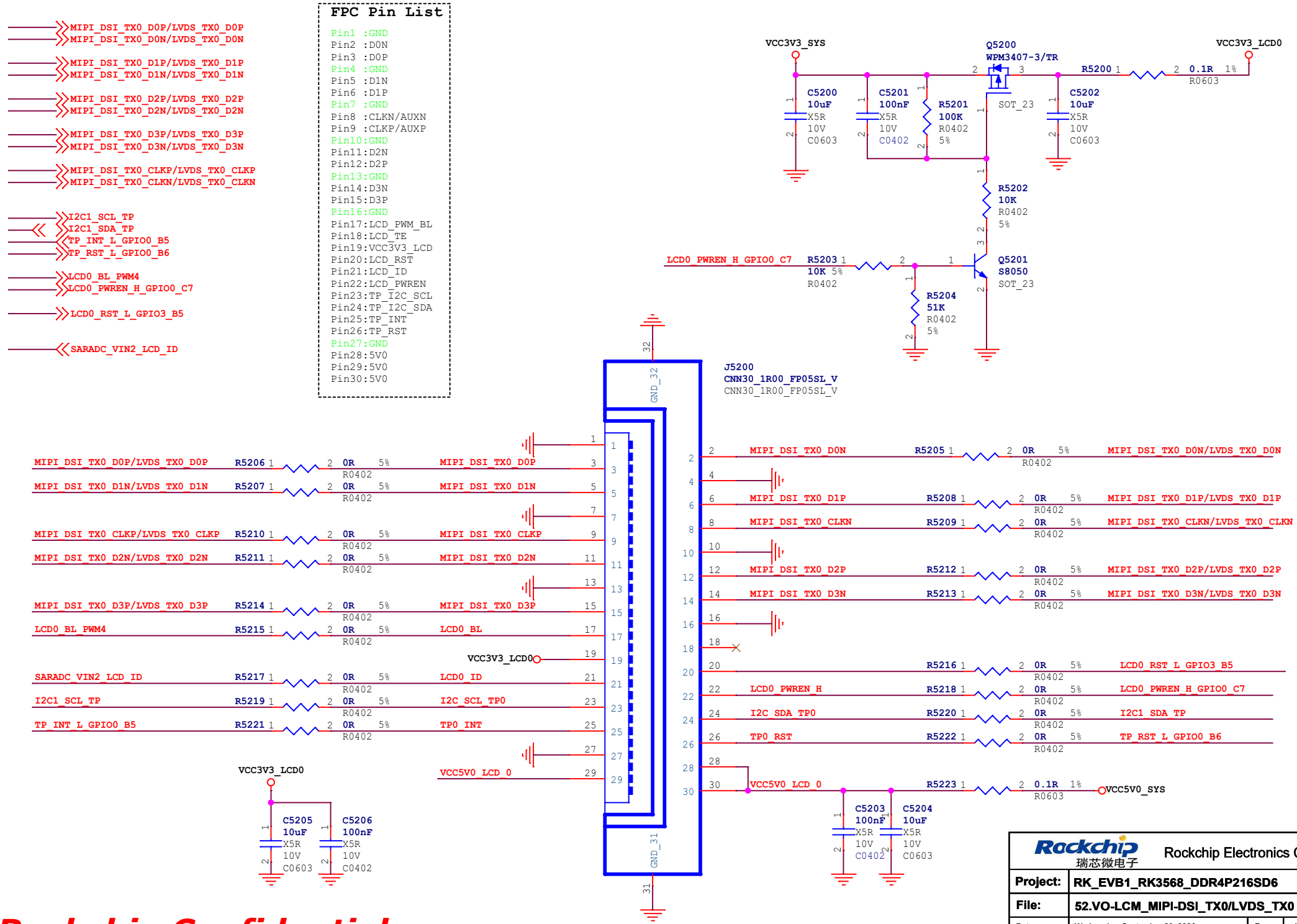
FPC Pin List
Pin1 :GND
Pin2 :D0N
Pin3 :D0P
Pin4 :GND
Pin5 :D1N
Pin6 :D1P
Pin7 :GND
Pin8 :CLKN/AUXN
Pin9 :CLKP/AUXP
Pin10:GND
Pin11:D2N
Pin12:D2P
Pin13:GND
Pin14:D3N
Pin15:D3P
Pin16:GND
Pin17:LCD_PWM_BL
Pin18:LCD_TE
Pin19:VCC3V3_LCD
Pin20:LCD_RST
Pin21:LCD_ID
Pin22:LCD_PWREN
Pin23:TP_I2C_SCL
Pin24:TP_I2C_SDA
Pin25:TP_INT
Pin26:TP_RST
Pin27:GND
Pin28:5V0
Pin29:5V0
Pin30:5V0
MIPI_DSI_TX0_D0P/LVDS_TX0_D0P
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP
MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN
I2C1_SCL_TP
I2C1_SDA_TP
TP_INT_L_GPIO0_B5
TP_RST_L_GPIO0_B6
LCD0_BL_PWM4
LCD0_PWREN_H_GPIO0_C7
LCD0_RST_L_GPIO3_B5
SARADC_VIN2_LCD_ID
VCC3V3_SYS
Q5200
WPM3407-3/TR
SOT_23
VCC3V3_LCD0
R5200 0.1R 1% R0603
C5200 10uF X5R 10V C0603
C5201 100nF X5R 10V C0402
R5201 100K R0402 5%
C5202 10uF X5R 10V C0603
R5202 10K R0402 5%
LCD0_PWREN_H_GPIO0_C7
R5203 10K 5% R0402
Q5201 S8050 SOT_23
R5204 51K R0402 5%
J5200
CNN30_1R00_FP05SL_V
GND_32
GND_31
MIPI_DSI_TX0_D0P/LVDS_TX0_D0P R5206 0R R0402 MIPI_DSI_TX0_D0P
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N R5207 0R R0402 MIPI_DSI_TX0_D1N
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP R5210 0R R0402 MIPI_DSI_TX0_CLKP
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N R5211 0R R0402 MIPI_DSI_TX0_D2N
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P R5214 0R R0402 MIPI_DSI_TX0_D3P
LCD0_BL_PWM4 R5215 0R R0402 LCD0_BL
VCC3V3_LCD0
SARADC_VIN2_LCD_ID R5217 0R R0402 LCD0_ID
I2C1_SCL_TP R5219 0R R0402 I2C_SCL_TP0
TP_INT_L_GPIO0_B5 R5221 0R R0402 TP0_INT
VCC5V0_LCD_0
MIPI_DSI_TX0_D0N R5205 0R R0402 MIPI_DSI_TX0_D0N/LVDS_TX0_D0N
MIPI_DSI_TX0_D1P R5208 0R R0402 MIPI_DSI_TX0_D1P/LVDS_TX0_D1P
MIPI_DSI_TX0_CLKN R5209 0R R0402 MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN
MIPI_DSI_TX0_D2P R5212 0R R0402 MIPI_DSI_TX0_D2P/LVDS_TX0_D2P
MIPI_DSI_TX0_D3N R5213 0R R0402 MIPI_DSI_TX0_D3N/LVDS_TX0_D3N
R5216 0R R0402 LCD0_RST_L_GPIO3_B5
LCD0_PWREN_H R5218 0R R0402 LCD0_PWREN_H_GPIO0_C7
I2C_SDA_TP0 R5220 0R R0402 I2C1_SDA_TP
TP0_RST R5222 0R R0402 TP_RST_L_GPIO0_B6
VCC5V0_LCD_0 R5223 0.1R 1% R0603 VCC5V0_SYS
C5205 10uF X5R 10V C0603
C5206 100nF X5R 10V C0402
C5203 100nF X5R 10V C0402
C5204 10uF X5R 10V C0603
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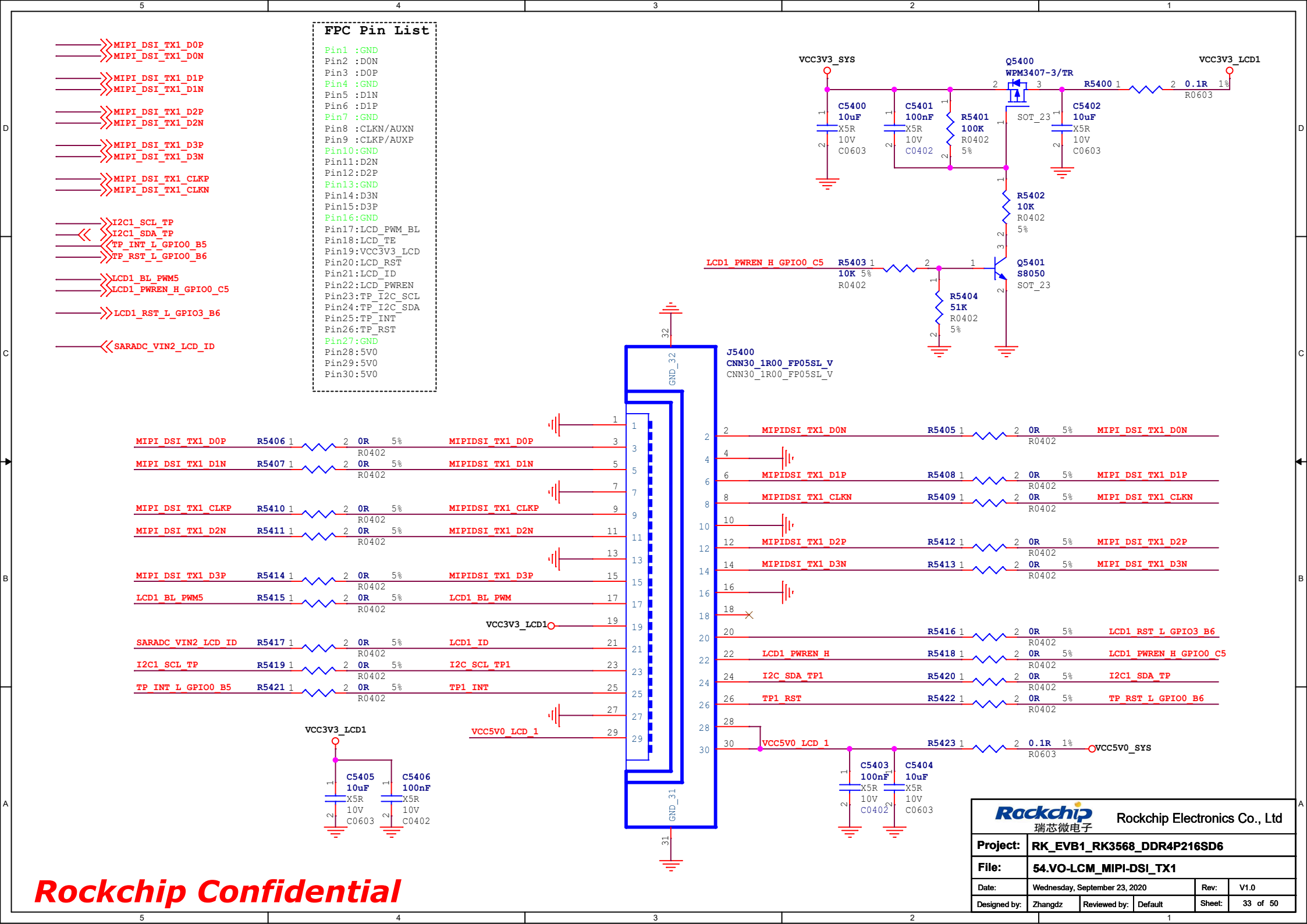
Rockchip Electronics Co., Ltd
Project: RK_EVB1_RK3568_DDR4P216SD6
File: 52.VO-LCM_MIPI-DSI_TX0/LVDS_TX0
Date: Wednesday, September 23, 2020
Rev: V1.0
Designed by: Zhangdz
Reviewed by: Default
Sheet: 32 of 50


MIPI_DSI_TX1_D0P
MIPI_DSI_TX1_D0N
MIPI_DSI_TX1_D1P
MIPI_DSI_TX1_D1N
MIPI_DSI_TX1_D2P
MIPI_DSI_TX1_D2N
MIPI_DSI_TX1_D3P
MIPI_DSI_TX1_D3N
MIPI_DSI_TX1_CLKP
MIPI_DSI_TX1_CLKN
I2C1_SCL_TP
I2C1_SDA_TP
TP_INT_L_GPIO0_B5
TP_RST_L_GPIO0_B6
LCD1_BL_PWM5
LCD1_PWREN_H_GPIO0_C5
LCD1_RST_L_GPIO3_B6
SARADC_VIN2_LCD_ID
FPC Pin List
Pin1 :GND
Pin2 :D0N
Pin3 :D0P
Pin4 :GND
Pin5 :D1N
Pin6 :D1P
Pin7 :GND
Pin8 :CLKN/AUXN
Pin9 :CLKP/AUXP
Pin10:GND
Pin11:D2N
Pin12:D2P
Pin13:GND
Pin14:D3N
Pin15:D3P
Pin16:GND
Pin17:LCD_PWM_BL
Pin18:LCD_TE
Pin19:VCC3V3_LCD
Pin20:LCD_RST
Pin21:LCD_ID
Pin22:LCD_PWREN
Pin23:TP_I2C_SCL
Pin24:TP_I2C_SDA
Pin25:TP_INT
Pin26:TP_RST
Pin27:GND
Pin28:5V0
Pin29:5V0
Pin30:5V0
VCC3V3_SYS
Q5400
WPM3407-3/TR
VCC3V3_LCD1
R5400 0.1R R0603
C5400 10uF X5R 10V C0603
C5401 100nF X5R 10V C0402
R5401 100K R0402 5%
C5402 10uF X5R 10V C0603
R5402 10K R0402 5%
LCD1_PWREN_H_GPIO0_C5
R5403 10K 5% R0402
Q5401 S8050 SOT_23
R5404 51K R0402 5%
J5400
CNN30_1R00_FP05SL_V
GND_32
GND_31
MIPI_DSI_TX1_D0P R5406 0R R0402 MIPIDSI_TX1_D0P
MIPI_DSI_TX1_D1N R5407 0R R0402 MIPIDSI_TX1_D1N
MIPI_DSI_TX1_CLKP R5410 0R R0402 MIPIDSI_TX1_CLKP
MIPI_DSI_TX1_D2N R5411 0R R0402 MIPIDSI_TX1_D2N
MIPI_DSI_TX1_D3P R5414 0R R0402 MIPIDSI_TX1_D3P
LCD1_BL_PWM5 R5415 0R R0402 LCD1_BL_PWM
VCC3V3_LCD1
SARADC_VIN2_LCD_ID R5417 0R R0402 LCD1_ID
I2C1_SCL_TP R5419 0R R0402 I2C_SCL_TP1
TP_INT_L_GPIO0_B5 R5421 0R R0402 TP1_INT
VCC5V0_LCD_1
MIPIDSI_TX1_D0N R5405 0R R0402 MIPI_DSI_TX1_D0N
MIPIDSI_TX1_D1P R5408 0R R0402 MIPI_DSI_TX1_D1P
MIPIDSI_TX1_CLKN R5409 0R R0402 MIPI_DSI_TX1_CLKN
MIPIDSI_TX1_D2P R5412 0R R0402 MIPI_DSI_TX1_D2P
MIPIDSI_TX1_D3N R5413 0R R0402 MIPI_DSI_TX1_D3N
R5416 0R R0402 LCD1_RST_L_GPIO3_B6
LCD1_PWREN_H R5418 0R R0402 LCD1_PWREN_H_GPIO0_C5
I2C_SDA_TP1 R5420 0R R0402 I2C1_SDA_TP
TP1_RST R5422 0R R0402 TP_RST_L_GPIO0_B6
VCC5V0_LCD_1 R5423 0.1R R0603 VCC5V0_SYS
C5403 100nF X5R 10V C0402
C5404 10uF X5R 10V C0603
C5405 10uF X5R 10V C0603
C5406 100nF X5R 10V C0402
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Rockchip 瑞芯微电子
Rockchip Electronics Co., Ltd
Project: RK_EVB1_RK3568_DDR4P216SD6
File: 54.VO-LCM_MIPI-DSI_TX1
Date: Wednesday, September 23, 2020
Rev: V1.0
Designed by: Zhangdz
Reviewed by: Default
Sheet: 33 of 50

EDP_TX_D0P
EDP_TX_D0N
EDP_TX_D1P
EDP_TX_D1N
EDP_TX_D2P
EDP_TX_D2N
EDP_TX_D3P
EDP_TX_D3N
EDP_TX_AUXP
EDP_TX_AUXN
I2C1_SCL_TP
I2C1_SDA_TP
TP_INT_L_GPIO0_B5
TP_RST_L_GPIO0_B6
LCD0_BL_PWM4
LCD0_PWREN_H_GPIO0_C7
LCD0_RST_L_GPIO3_B5
SARADC_VIN2_LCD_ID

VCC_1V8
Q5600 2SK3018 SOT_323
R5600 2.2K 5% R0402 DNP
3.3V
I2C1_SCL_TP
I2C1_SCL_TP_CON
R5602 DNP 0R 5% R0402
1.8V

VCC_1V8
Q5601 2SK3018 SOT_323
R5601 2.2K 5% R0402 DNP
3.3V
I2C1_SDA_TP
I2C1_SDA_TP_CON
R5603 DNP 0R 5% R0402

3.3V
TP_INT_L_GPIO0_B5
R5604 0R 5% R0402
TP_INT_L_GPIO0_B5_CON

3.3V
TP_RST_L_GPIO0_B6
R5605 0R 5% R0402
TP_RST_L_GPIO0_B6_CON

For Debug

Default: eDP to VGA
Place at branch point

J5600
CNN30_1R00_FP05SL_V
CNN30_1R00_FP05SL_V

EDP_TX_D0P R5606 DNP 0R 5% R0201 EDP_TX_D0P_CON
EDP_TX_D1N R5607 DNP 0R 5% R0201 EDP_TX_D1N_CON
VCC3V3_LCD0 R5608 100K 5% R0402
EDP_TX_AUXN C5600 100nF X5R 10V C0402 DNP
EDP_TX_AUXP C5601 100nF X5R 10V C0402 DNP
EDP_TX_AUXN_CON
R5611 100K 5% R0402
EDP_TX_AUXP_CON
EDP_TX_D2N R5612 0R 5% R0201 EDP_TX_D2N_CON
EDP_TX_D3P R5615 0R 5% R0201 EDP_TX_D3P_CON
LCD0_BL_PWM4 R5616 0R 5% R0402
VCC3V3_LCD0
SARADC_VIN2_LCD_ID R5618 0R 5% R0402
I2C1_SCL_TP_CON
TP_INT_L_GPIO0_B5_CON

EDP_TX_D0N_CON R5609 DNP 0R 5% R0201 EDP_TX_D0N
EDP_TX_D1P_CON R5610 DNP 0R 5% R0201 EDP_TX_D1P
EDP_TX_AUXN_CON
EDP_TX_D2P_CON R5613 0R 5% R0201 EDP_TX_D2P
EDP_TX_D3N_CON R5614 0R 5% R0201 EDP_TX_D3N
R5617 0R 5% R0402 LCD0_RST_L_GPIO3_B5
R5619 0R 5% R0402 LCD0_PWREN_H_GPIO0_C7
I2C1_SDA_TP_CON
TP_RST_L_GPIO0_B6_CON
VCC5V0_LCDEDP

GND_32
GND_31

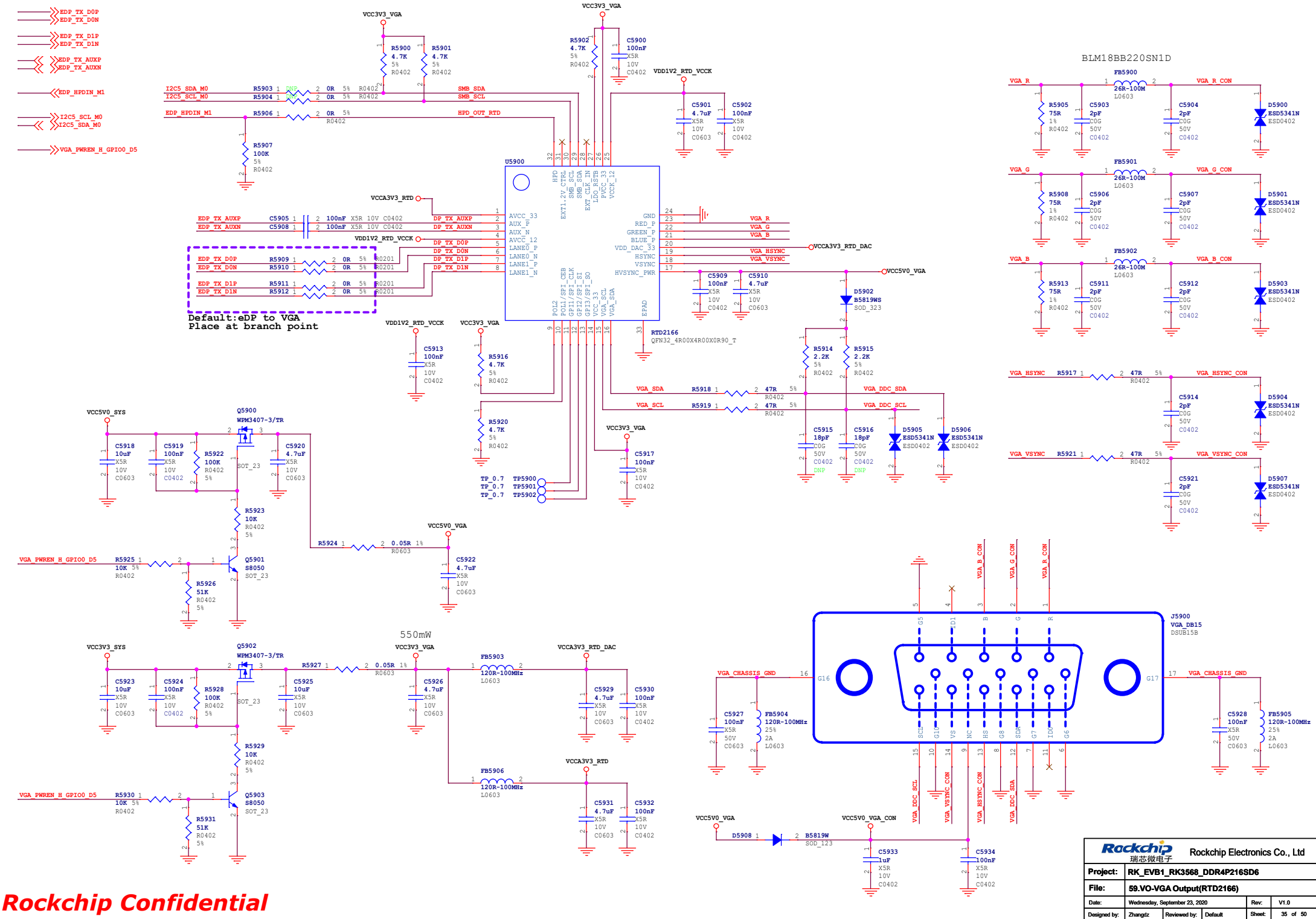
VCC3V3_LCD0
C5602 10uF X5R 10V C0603
C5603 100nF X5R 10V C0402

VCC5V0_SYS
R5620 0.1R 1% R0603
VCC5V0_LCDEDP
C5604 10uF X5R 10V C0603
C5605 100nF X5R 10V C0402

FPC Pin List

Pin1 :GND
Pin2 :D0N
Pin3 :D0P
Pin4 :GND
Pin5 :D1N
Pin6 :D1P
Pin7 :GND
Pin8 :CLKN/AUXN
Pin9 :CLKP/AUXP
Pin10:GND
Pin11:D2N
Pin12:D2P
Pin13:GND
Pin14:D3N
Pin15:D3P
Pin16:GND
Pin17:LCD_PWM_BL
Pin18:LCD_TE
Pin19:VCC3V3_LCD
Pin20:LCD_RST
Pin21:LCD_ID
Pin22:LCD_PWREN
Pin23:TP_I2C_SCL
Pin24:TP_I2C_SDA
Pin25:TP_INT
Pin26:TP_RST
Pin27:GND
Pin28:5V0
Pin29:5V0
Pin30:5V0

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	56.VO-LCM_eDP(Option)				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	34 of 50



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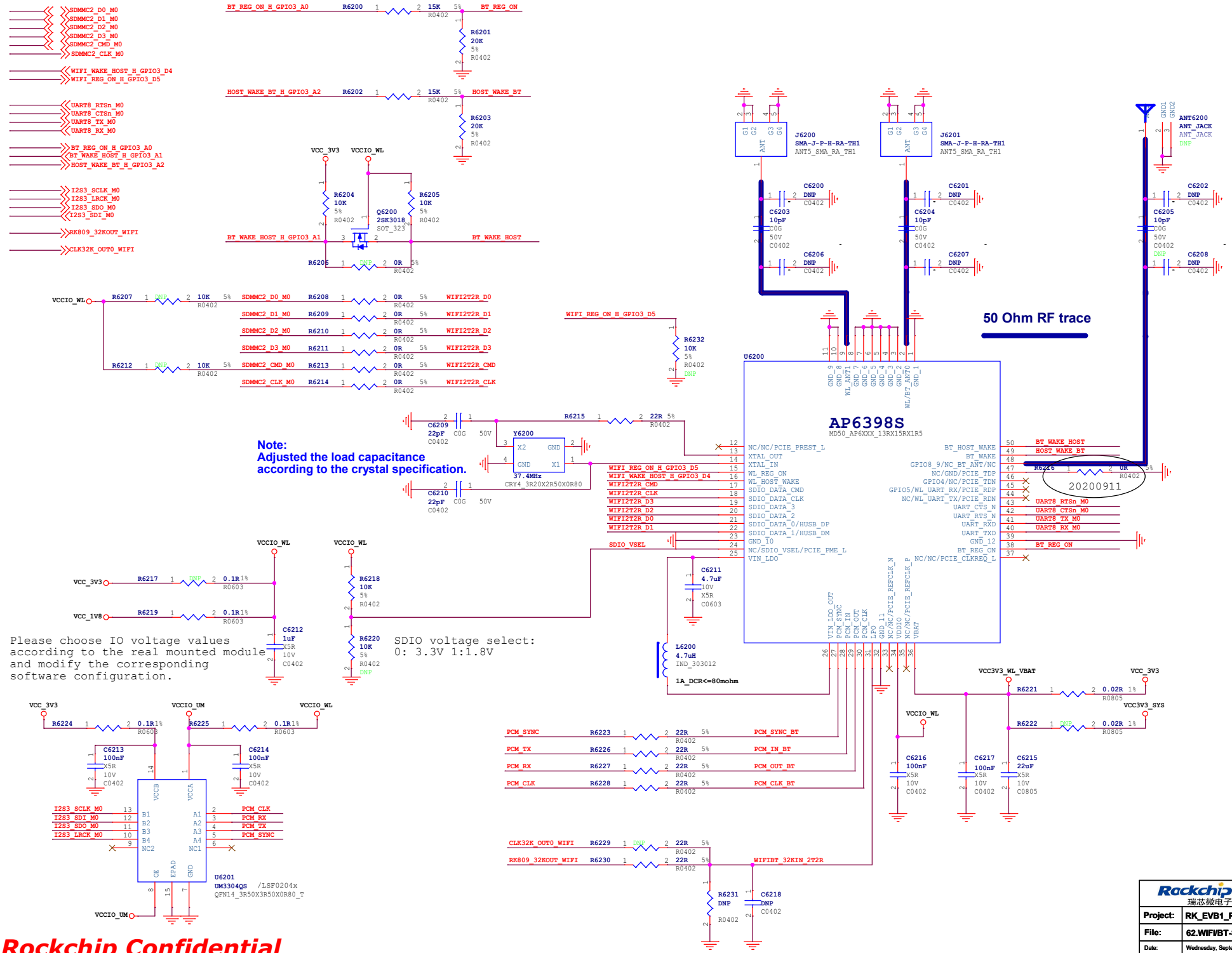
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	59.VO-VGA Output(RTD2166)				
Date:	Wednesday, September 23, 2020		Rev:	V1.0	
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	35 of 50



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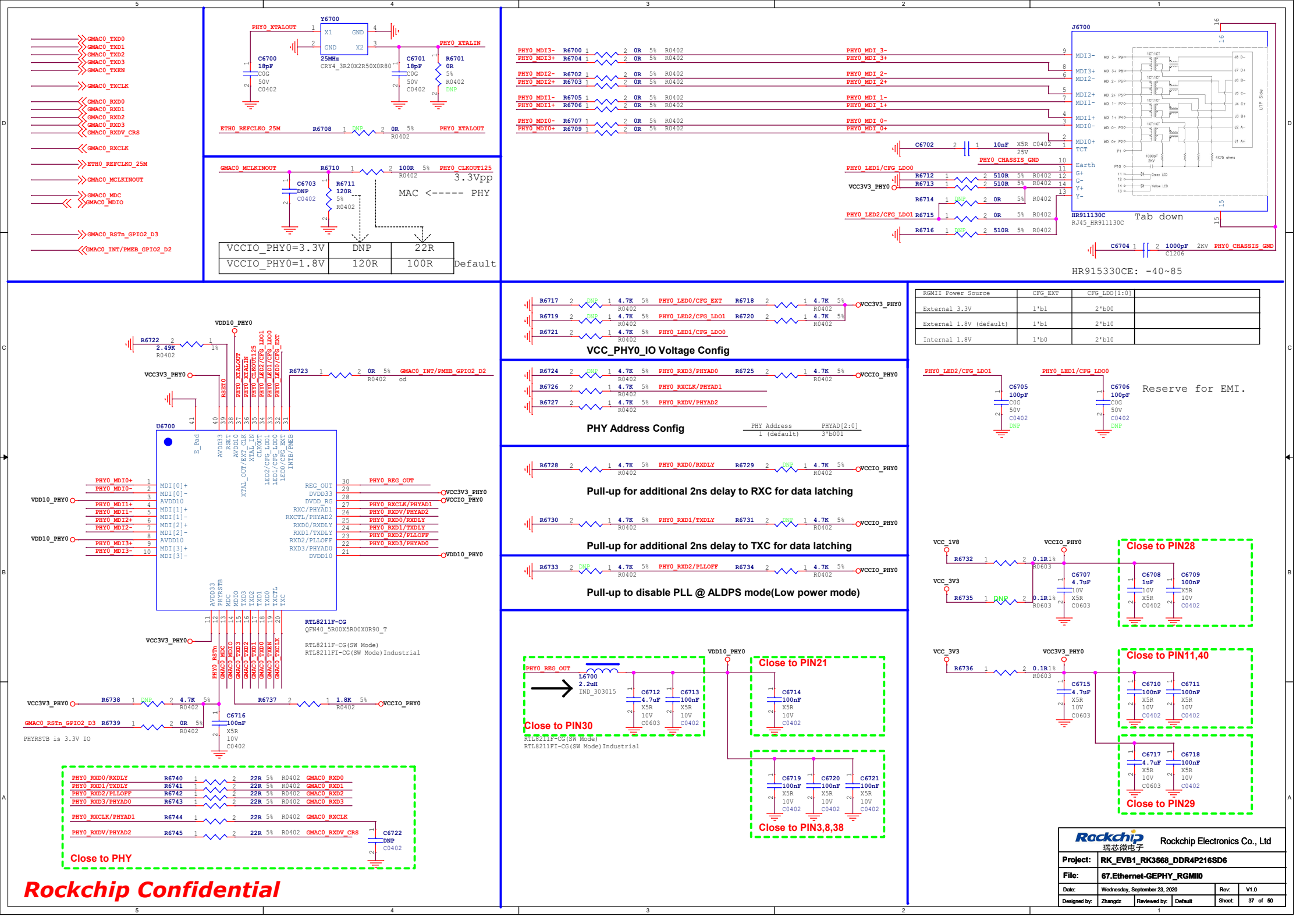
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	62.WIFI/BT-SDIO_2T2R + UART				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	36 of 50


GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
ETH0_REFCLKO_25M
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
GMAC0_RSTn_GPIO2_D3
GMAC0_INT/PMEB_GPIO2_D2
Y6700
PHY0_XTALOUT
PHY0_XTALIN
25MHz
CRY4_3R20X2R50X0R80
C6700 18pF C0G 50V C0402
C6701 18pF C0G 50V C0402
R6701 0R 5% R0402 DNP
ETH0_REFCLKO_25M
R6708 DNP 0R 5% R0402
GMAC0_MCLKINOUT
R6710 100R 5% R0402
PHY0_CLKOUT125
3.3Vpp
MAC <----- PHY
C6703 DNP C0402
R6711 120R 5% R0402
VCCIO_PHY0=3.3V DNP 22R
VCCIO_PHY0=1.8V 120R 100R Default
PHY0_MDI3- R6700 0R R0402
PHY0_MDI3+ R6704 0R R0402
PHY0_MDI2- R6702 0R R0402
PHY0_MDI2+ R6703 0R R0402
PHY0_MDI1- R6705 0R R0402
PHY0_MDI1+ R6706 0R R0402
PHY0_MDI0- R6707 0R R0402
PHY0_MDI0+ R6709 0R R0402
PHY0_MDI_3-
PHY0_MDI_3+
PHY0_MDI_2-
PHY0_MDI_2+
PHY0_MDI_1-
PHY0_MDI_1+
PHY0_MDI_0-
PHY0_MDI_0+
J6700
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
TCT
Earth
G+
G-
Y+
Y-
C6702 10nF X5R C0402 25V
PHY0_CHASSIS_GND
PHY0_LED1/CFG_LDO0
R6712 510R 5% R0402
R6713 510R 5% R0402
VCC3V3_PHY0
R6714 DNP 0R 5% R0402
PHY0_LED2/CFG_LDO1
R6715 0R 5% R0402
R6716 DNP 510R 5% R0402
HR911130C
RJ45_HR911130C
Tab down
C6704 1000pF 2KV C1206
PHY0_CHASSIS_GND
HR915330CE: -40~85
VDD10_PHY0
R6722 2.49K 1% R0402
VCC3V3_PHY0
R6723 0R 5% R0402 od
GMAC0_INT/PMEB_GPIO2_D2
RSET0
PHY0_XTALOUT
PHY0_XTALIN
PHY0_CLKOUT125
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
PHY0_LED0/CFG_EXT
U6700
E_Pad
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INT#/PMEB
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY0_REG_OUT
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
PHY0_RSTn
GMAC0_MDC
GMAC0_MDIO
GMAC0_TXD3
GMAC0_TXD2
GMAC0_TXD1
GMAC0_TXD0
GMAC0_TXEN
GMAC0_TXCLK
R6738 DNP 4.7K R0402
R6737 1.8K R0402
VCCIO_PHY0
GMAC0_RSTn_GPIO2_D3 R6739 0R R0402
PHYRSTB is 3.3V IO
C6716 100nF X5R 10V C0402
PHY0_RXD0/RXDLY R6740 22R R0402 GMAC0_RXD0
PHY0_RXD1/TXDLY R6741 22R R0402 GMAC0_RXD1
PHY0_RXD2/PLLOFF R6742 22R R0402 GMAC0_RXD2
PHY0_RXD3/PHYAD0 R6743 22R R0402 GMAC0_RXD3
PHY0_RXCLK/PHYAD1 R6744 22R R0402 GMAC0_RXCLK
PHY0_RXDV/PHYAD2 R6745 22R R0402 GMAC0_RXDV_CRS
C6722 DNP C0402
Close to PHY
R6717 DNP 4.7K R0402 PHY0_LED0/CFG_EXT
R6718 4.7K R0402
R6719 DNP 4.7K R0402 PHY0_LED2/CFG_LDO1
R6720 4.7K R0402
R6721 4.7K R0402 PHY0_LED1/CFG_LDO0
VCC_PHY0_IO Voltage Config
R6724 DNP 4.7K R0402 PHY0_RXD3/PHYAD0
R6725 4.7K R0402
R6726 4.7K R0402 PHY0_RXCLK/PHYAD1
R6727 4.7K R0402 PHY0_RXDV/PHYAD2
PHY Address Config
PHY Address 1 (default)
PHYAD[2:0] 3'b001
R6728 4.7K R0402 PHY0_RXD0/RXDLY
R6729 DNP 4.7K R0402
Pull-up for additional 2ns delay to RXC for data latching
R6730 4.7K R0402 PHY0_RXD1/TXDLY
R6731 DNP 4.7K R0402
Pull-up for additional 2ns delay to TXC for data latching
R6733 DNP 4.7K R0402 PHY0_RXD2/PLLOFF
R6734 4.7K R0402
Pull-up to disable PLL @ ALDPS mode(Low power mode)
PHY0_REG_OUT
L6700 2.2uH IND_303015
C6712 4.7uF X5R 10V C0603
C6713 100nF X5R 10V C0402
C6714 100nF X5R 10V C0402
Close to PIN21
Close to PIN30
C6719 100nF X5R 10V C0402
C6720 100nF X5R 10V C0402
C6721 100nF X5R 10V C0402
Close to PIN3,8,38
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V (default) | 1'b1 | 2'b10
Internal 1.8V | 1'b0 | 2'b10
PHY0_LED2/CFG_LDO1
C6705 100pF C0G 50V C0402 DNP
PHY0_LED1/CFG_LDO0
C6706 100pF C0G 50V C0402 DNP
Reserve for EMI.
VCC_1V8
R6732 0.1R 1% R0603
VCCIO_PHY0
C6707 4.7uF X5R 10V C0603
C6708 1uF X5R 10V C0402
C6709 100nF X5R 10V C0402
Close to PIN28
VCC_3V3
R6735 DNP 0.1R 1% R0603
VCC_3V3
R6736 0.1R 1% R0603
VCC3V3_PHY0
C6715 4.7uF X5R 10V C0603
C6710 100nF X5R 10V C0402
C6711 100nF X5R 10V C0402
Close to PIN11,40
C6717 4.7uF X5R 10V C0603
C6718 100nF X5R 10V C0402
Close to PIN29
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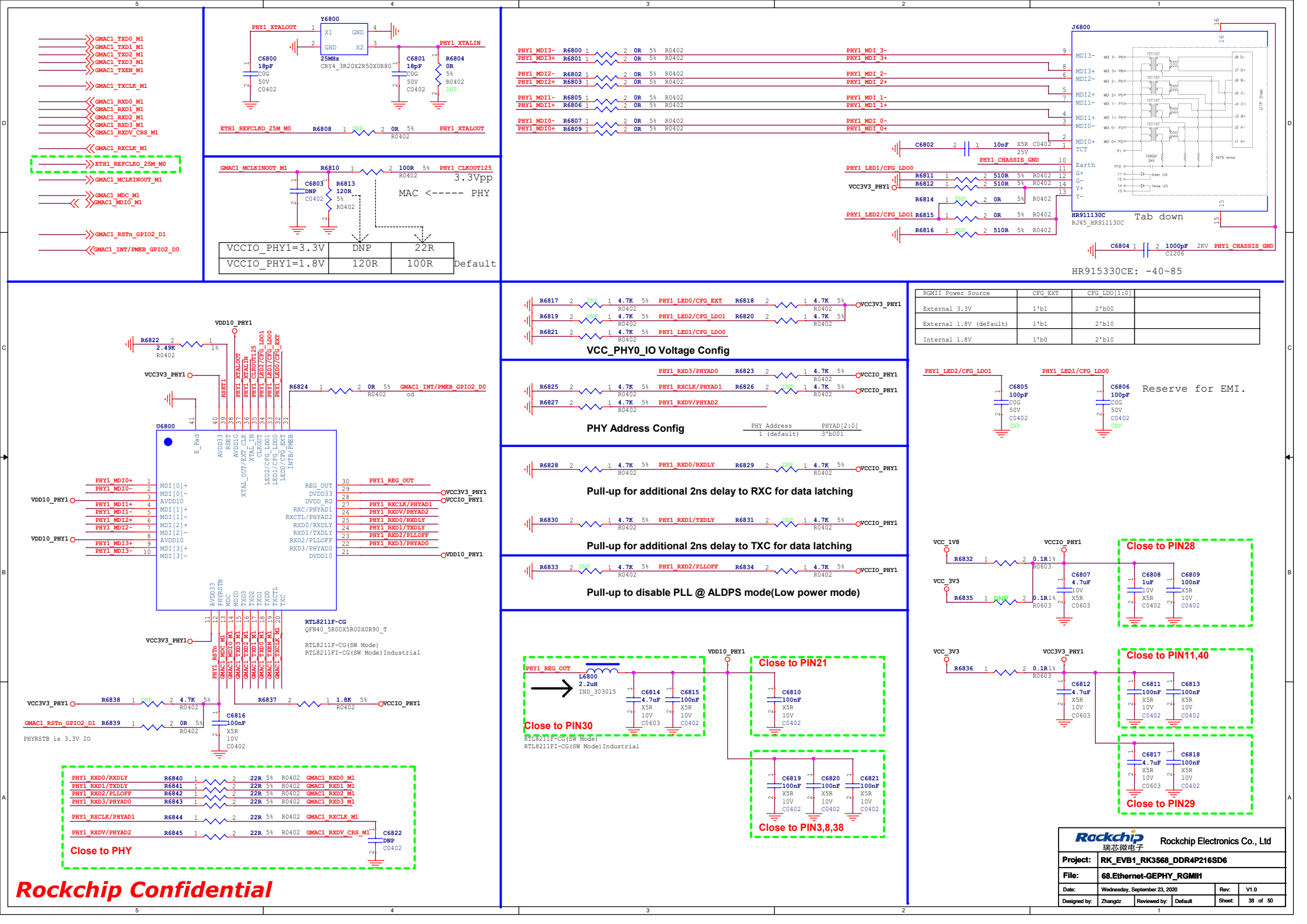
Project: RK_EVB1_RK3568_DDR4P216SD6
File: 67.Ethernet-GEPHY_RGMII0
Date: Wednesday, September 23, 2020
Rev: V1.0
Designed by: Zhangdz
Reviewed by: Default
Sheet: 37 of 50


GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXDV_CRS_M1
GMAC1_RXCLK_M1
ETH1_REFCLKO_25M_M0
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO2_D1
GMAC1_INT/PMEB_GPIO2_D0
Y6800
PHY1_XTALOUT
PHY1_XTALIN
C6800 18pF C0G 50V C0402
25MHz CRY4_3R20X2R50X0R80
C6801 18pF C0G 50V C0402
R6804 0R 5% R0402 DNP
ETH1_REFCLKO_25M_M0 R6808 DNP 0R 5% R0402 PHY1_XTALOUT
GMAC1_MCLKINOUT_M1 R6810 100R 5% R0402 PHY1_CLKOUT125
C6803 DNP C0402
R6813 120R 5% R0402
3.3Vpp
MAC <----- PHY
VCCIO_PHY1=3.3V DNP 22R
VCCIO_PHY1=1.8V 120R 100R Default
PHY1_MDI3- R6800 0R R0402 PHY1_MDI_3-
PHY1_MDI3+ R6801 0R R0402 PHY1_MDI_3+
PHY1_MDI2- R6802 0R R0402 PHY1_MDI_2-
PHY1_MDI2+ R6803 0R R0402 PHY1_MDI_2+
PHY1_MDI1- R6805 0R R0402 PHY1_MDI_1-
PHY1_MDI1+ R6806 0R R0402 PHY1_MDI_1+
PHY1_MDI0- R6807 0R R0402 PHY1_MDI_0-
PHY1_MDI0+ R6809 0R R0402 PHY1_MDI_0+
C6802 10nF X5R C0402 25V
PHY1_CHASSIS_GND
PHY1_LED1/CFG_LDO0
VCC3V3_PHY1
R6811 510R 5% R0402
R6812 510R 5% R0402
R6814 DNP 0R 5% R0402
PHY1_LED2/CFG_LDO1 R6815 0R 5% R0402
R6816 DNP 510R 5% R0402
J6800
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
TCT
Earth
G+
G-
Y+
Y-
HR911130C
RJ45_HR911130C
Tab down
C6804 1000pF 2KV C1206
PHY1_CHASSIS_GND
HR915330CE: -40~85
VDD10_PHY1
R6822 2.49K R0402
VCC3V3_PHY1
R6824 0R 5% R0402 GMAC1_INT/PMEB_GPIO2_D0 od
U6800
E_Pad
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY1_REG_OUT
VCC3V3_PHY1
VCCIO_PHY1
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
PHY1_RXD0/RXDLY
PHY1_RXD1/TXDLY
PHY1_RXD2/PLLOFF
PHY1_RXD3/PHYAD0
VDD10_PHY1
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
RTL8211F-CG
QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
VCC3V3_PHY1
R6838 DNP 4.7K R0402
R6837 1.8K R0402 VCCIO_PHY1
GMAC1_RSTn_GPIO2_D1 R6839 0R R0402
PHYRSTB is 3.3V IO
C6816 100nF X5R 10V C0402
PHY1_RXD0/RXDLY R6840 22R R0402 GMAC1_RXD0_M1
PHY1_RXD1/TXDLY R6841 22R R0402 GMAC1_RXD1_M1
PHY1_RXD2/PLLOFF R6842 22R R0402 GMAC1_RXD2_M1
PHY1_RXD3/PHYAD0 R6843 22R R0402 GMAC1_RXD3_M1
PHY1_RXCLK/PHYAD1 R6844 22R R0402 GMAC1_RXCLK_M1
PHY1_RXDV/PHYAD2 R6845 22R R0402 GMAC1_RXDV_CRS_M1
C6822 DNP C0402
Close to PHY
R6817 DNP 4.7K R0402 PHY1_LED0/CFG_EXT R6818 4.7K R0402 VCC3V3_PHY1
R6819 DNP 4.7K R0402 PHY1_LED2/CFG_LDO1 R6820 4.7K R0402
R6821 4.7K R0402 PHY1_LED1/CFG_LDO0
VCC_PHY0_IO Voltage Config
R6825 4.7K R0402 PHY1_RXD3/PHYAD0 R6823 4.7K R0402 VCCIO_PHY1
R6827 4.7K R0402 PHY1_RXCLK/PHYAD1 R6826 DNP 4.7K R0402 VCCIO_PHY1
PHY1_RXDV/PHYAD2
PHY Address Configuration
PHY Address PHYAD[2:0]
1 (default) 3'b001
R6828 4.7K R0402 PHY1_RXD0/RXDLY R6829 DNP 4.7K R0402 VCCIO_PHY1
Pull-up for additional 2ns delay to RXC for data latching
R6830 4.7K R0402 PHY1_RXD1/TXDLY R6831 DNP 4.7K R0402 VCCIO_PHY1
Pull-up for additional 2ns delay to TXC for data latching
R6833 DNP 4.7K R0402 PHY1_RXD2/PLLOFF R6834 4.7K R0402 VCCIO_PHY1
Pull-up to disable PLL @ ALDPS mode(Low power mode)
VDD10_PHY1
PHY1_REG_OUT
L6800 2.2uH IND_303015
C6814 4.7uF X5R 10V C0603
C6815 100nF X5R 10V C0402
Close to PIN30
C6810 100nF X5R 10V C0402
Close to PIN21
C6819 100nF X5R 10V C0402
C6820 100nF X5R 10V C0402
C6821 100nF X5R 10V C0402
Close to PIN3,8,38
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
RGMII Power Source | CFG_EXT | CFG_LDO[1:0]
External 3.3V | 1'b1 | 2'b00
External 1.8V (default) | 1'b1 | 2'b10
Internal 1.8V | 1'b0 | 2'b10
PHY1_LED2/CFG_LDO1
C6805 100pF C0G 50V C0402 DNP
PHY1_LED1/CFG_LDO0
C6806 100pF C0G 50V C0402 DNP
Reserve for EMI.
VCC_1V8
R6832 0.1R 1% R0603
VCCIO_PHY1
C6807 4.7uF 10V X5R C0603
C6808 1uF 10V X5R C0402
C6809 100nF X5R 10V C0402
Close to PIN28
VCC_3V3
R6835 DNP 0.1R 1% R0603
R6836 0.1R 1% R0603
C6812 4.7uF X5R 10V C0603
C6811 100nF X5R 10V C0402
C6813 100nF X5R 10V C0402
Close to PIN11,40
C6817 4.7uF X5R 10V C0603
C6818 100nF X5R 10V C0402
Close to PIN29
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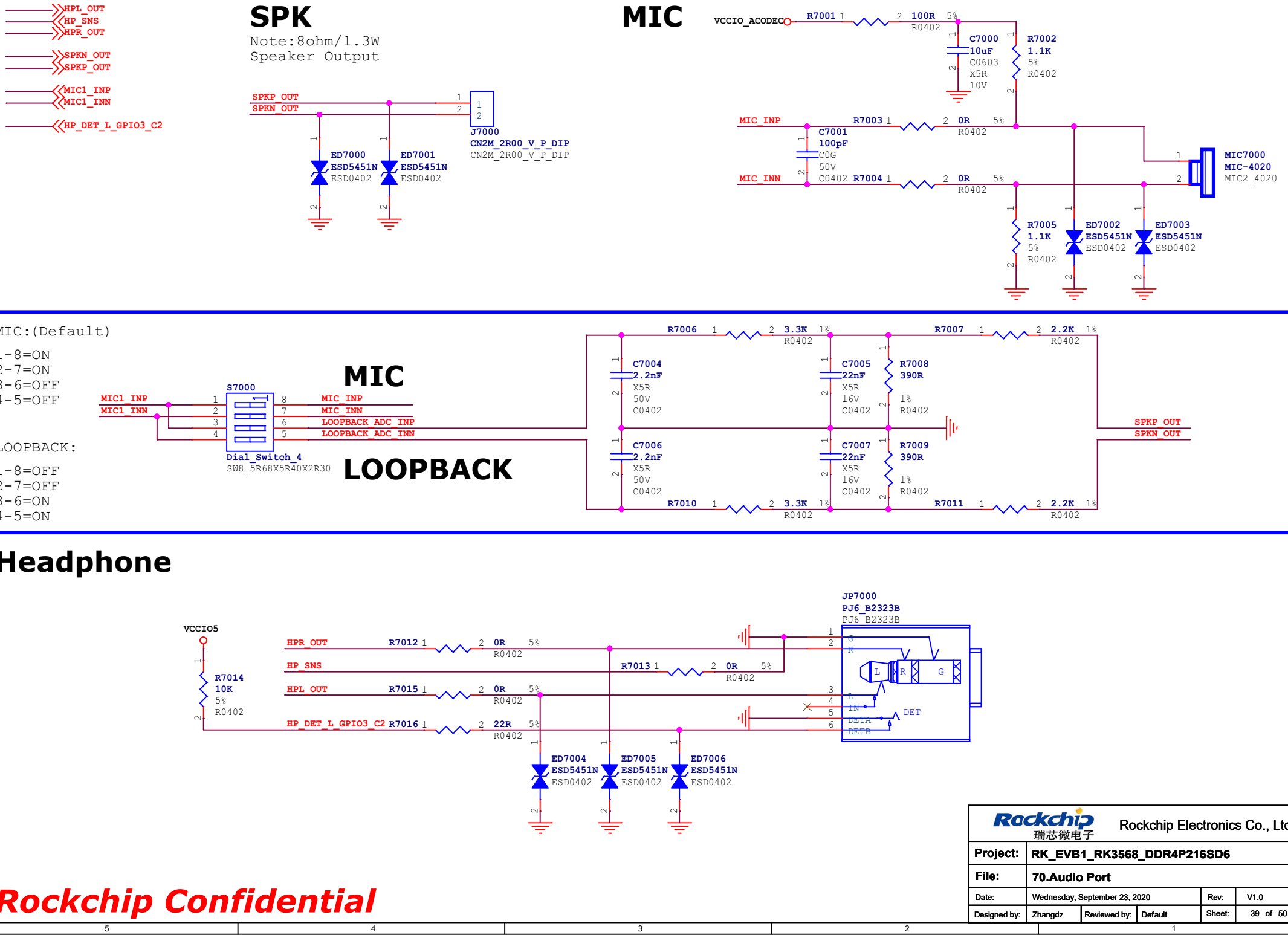
Rockchip Electronics Co., Ltd
Project: RK_EVB1_RK3568_DDR4P216SD6
File: 68.Ethernet-GEPHY_RGMII
Date: Wednesday, September 23, 2020
Rev: V1.0
Designed by: Zhangdz
Reviewed by: Default
Sheet: 38 of 50


HPL_OUT
HP_SNS
HPR_OUT
SPKN_OUT
SPKP_OUT
MIC1_INP
MIC1_INN
HP_DET_L_GPIO3_C2
SPK
Note:8ohm/1.3W
Speaker Output
SPKP_OUT
SPKN_OUT
J7000
CN2M_2R00_V_P_DIP
ED7000
ESD5451N
ESD0402
ED7001
ESD5451N
ESD0402
MIC
VCCIO_ACODEC
R7001 100R 5% R0402
C7000 10uF C0603 X5R 10V
R7002 1.1K 5% R0402
MIC_INP
R7003 0R 5% R0402
C7001 100pF C0G 50V C0402
MIC_INN
R7004 0R 5% R0402
MIC7000
MIC-4020
MIC2_4020
R7005 1.1K 5% R0402
ED7002 ESD5451N ESD0402
ED7003 ESD5451N ESD0402
MIC:(Default)
1-8=ON
2-7=ON
3-6=OFF
4-5=OFF
LOOPBACK:
1-8=OFF
2-7=OFF
3-6=ON
4-5=ON
MIC
S7000
MIC1_INP
MIC1_INN
MIC_INP
MIC_INN
LOOPBACK_ADC_INP
LOOPBACK_ADC_INN
Dial_Switch_4
SW8_5R68X5R40X2R30
LOOPBACK
R7006 3.3K 1% R0402
R7007 2.2K 1% R0402
C7004 2.2nF X5R 50V C0402
C7005 22nF X5R 16V C0402
R7008 390R 1% R0402
C7006 2.2nF X5R 50V C0402
C7007 22nF X5R 16V C0402
R7009 390R 1% R0402
R7010 3.3K 1% R0402
R7011 2.2K 1% R0402
SPKP_OUT
SPKN_OUT
Headphone
VCCIO5
R7014 10K 5% R0402
HPR_OUT
R7012 0R 5% R0402
HP_SNS
R7013 0R 5% R0402
HPL_OUT
R7015 0R 5% R0402
HP_DET_L_GPIO3_C2
R7016 22R 5% R0402
JP7000
PJ6_B2323B
DET
ED7004 ESD5451N ESD0402
ED7005 ESD5451N ESD0402
ED7006 ESD5451N ESD0402
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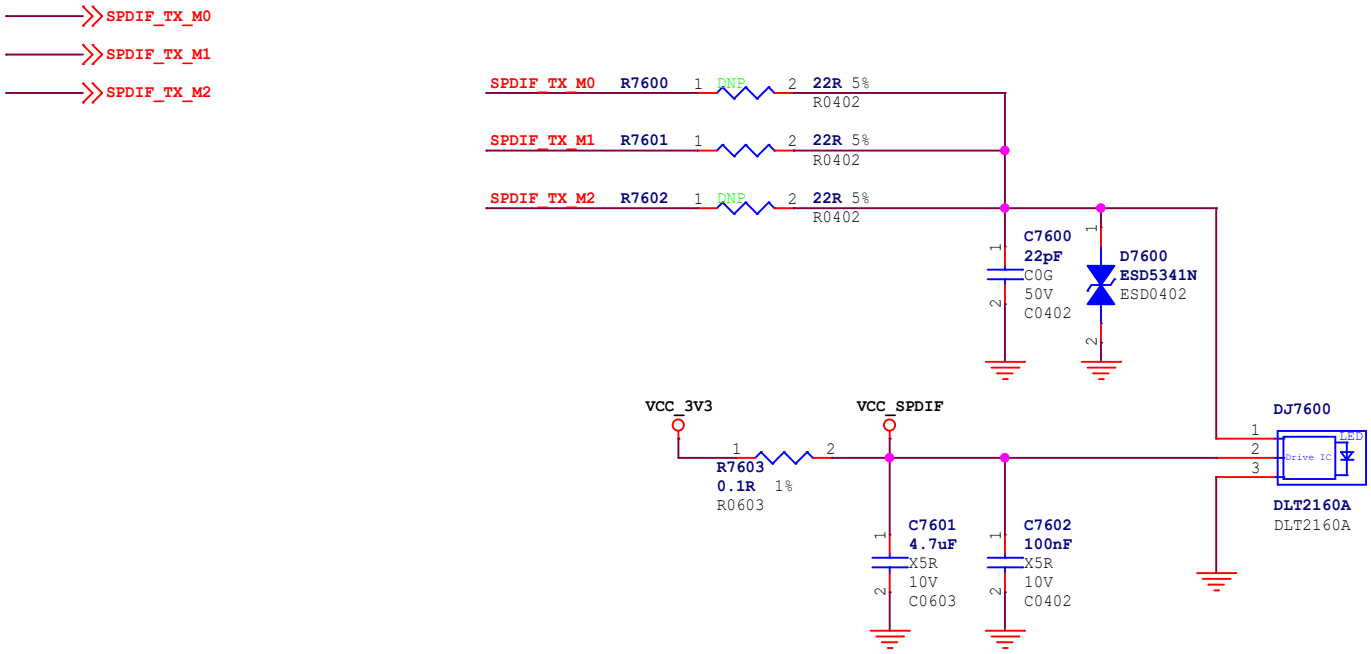
Rockchip 瑞芯微电子
Rockchip Electronics Co., Ltd
Project: RK_EVB1_RK3568_DDR4P216SD6
File: 70.Audio Port
Date: Wednesday, September 23, 2020
Rev: V1.0
Designed by: Zhangdz
Reviewed by: Default
Sheet: 39 of 50



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	76.Audio-S/PDIF TX Port				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	40 of 50

I2S1_MCLK_M0_CON

I2S1_SCLK_RX_M0/PDM_CLK1_M0_CON
I2S1_SCLK_TX_M0_CON

I2S1_LRCK_TX_M0_CON
I2S1_LRCK_RX_M0/PDM_CLK0_M0_CON

I2S1_SDO0_M0_CON
I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0_CON
I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0_CON
I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0_CON
I2S1_SDI0_M0/PDM_SDI0_M0_CON

I2C3_SDA_M0
I2C3_SCL_M0

HP_DET_L_GPIO3_C2

PA_EN_H_GPIO3_C3

VCCIO1
C7700 100nF X5R 10V C0402
C7701 10uF X5R 10V C0603
R7700 1 2 0.1R 1% R0603

VCC5V0_SYS
C7702 100nF X5R 10V C0402
C7703 10uF X5R 10V C0603
R7701 1 2 0.02R 1% R0805

VCC_3V3
C7704 100nF X5R 10V C0402
C7705 10uF X5R 10V C0603
R7702 1 2 0.1R 1% R0603

JP7700

1	VCC_5V_0	VCC_5V_1	2
3	VCCIO	GND0	4
5	GND1	VCC_3V3	6
7	GND2	Codec_EN/GPIO_A_d	8
9	GND3	I2S_MCLK	10
11	GND4	I2S_SCLK_RX/PDM_CLK1	12
13	GND5	I2S_SCLK_TX	14
15	GND6	I2S_LRCK_RX/PDM_CLK0	16
17	GND7	I2S_LRCK_TX	18
19	I2S_SDO0	I2S_SDO1	20
21	I2S_SDO2	I2S_SDO3	22
23	I2S_SDI0/PDM_SDI0	I2S_SDI1/PDM_SDI1	24
25	I2S_SDI2/PDM_SDI2	I2S_SDI3/PDM_SDI3	26
27	GND8	PA_EN/GPIO_B_d	28
29	I2C_SDA	I2C_SCL	30
		M_GND1	31
		M_GND2	32

1 Pin
0.5pitch
finger touch side

Connector of
Audio Extended Board
(Mainboard Side)

DigitalAudio_FFC_CON
CNN30_1R00_FP05SL_V

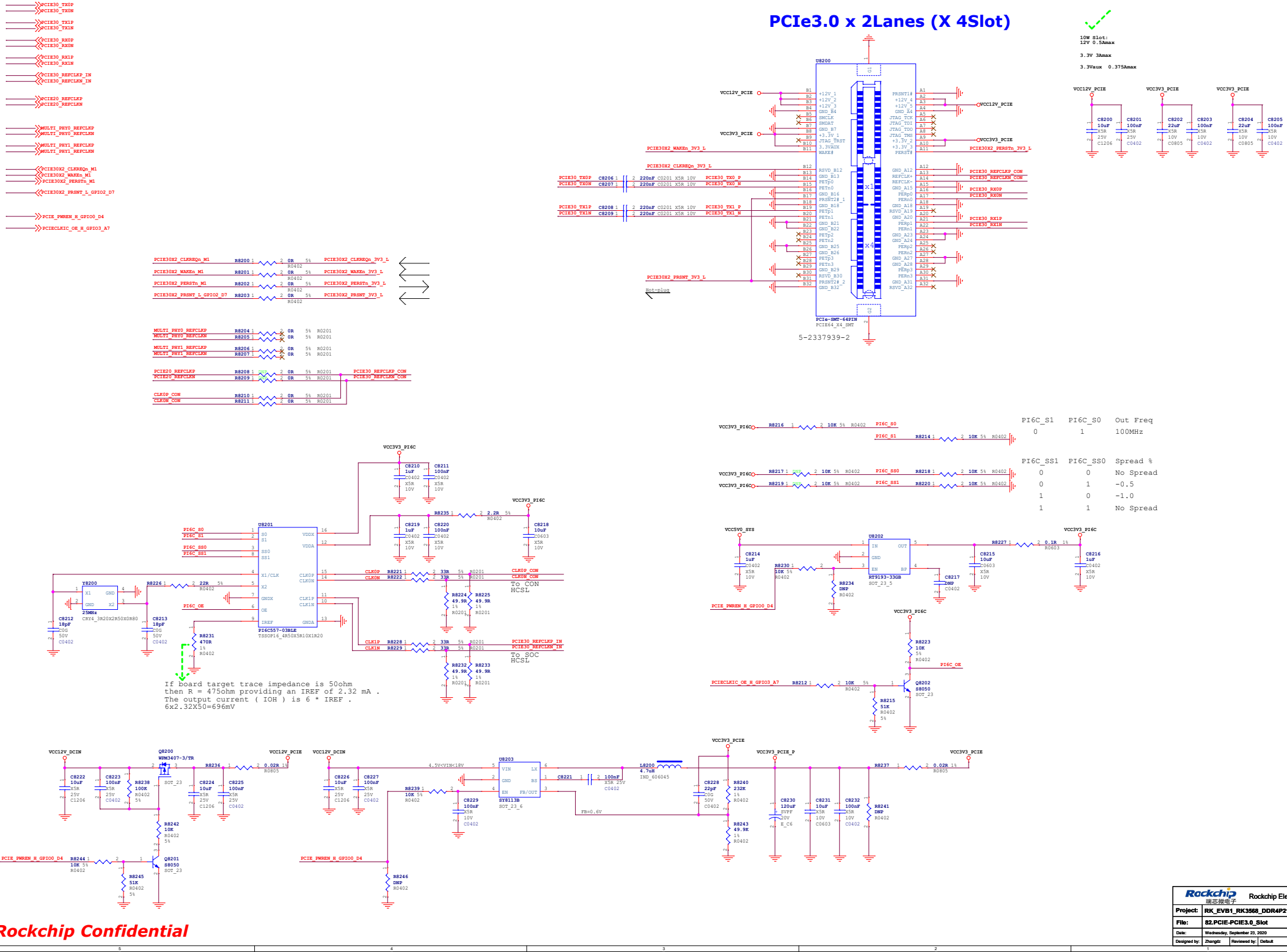
I2S1_SDO0_M0_CON — R7709 1 2 22R 5% R0402 — 19
I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0_CON — R7711 1 DNP 2 22R 5% R0402 — 21
I2S1_SDI0_M0/PDM_SDI0_M0_CON — R7713 1 2 22R 5% R0402 — 23
I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0_CON — R7715 1 2 22R 5% R0402 — 25
I2C3_SDA_M0 — R7718 1 2 22R 5% R0402 — 29

R7703 1 2 22R 5% R0402 — HP_DET_L_GPIO3_C2
R7704 1 2 22R 5% R0402 — I2S1_MCLK_M0_CON
R7705 1 2 22R 5% R0402 — I2S1_SCLK_RX_M0/PDM_CLK1_M0_CON
R7706 1 2 22R 5% R0402 — I2S1_SCLK_TX_M0_CON
R7707 1 2 22R 5% R0402 — I2S1_LRCK_RX_M0/PDM_CLK0_M0_CON
R7708 1 2 22R 5% R0402 — I2S1_LRCK_TX_M0_CON
R7710 1 DNP 2 22R 5% R0402 — I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0_CON
R7712 1 DNP 2 22R 5% R0402 — I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0_CON
R7714 1 2 22R 5% R0402 — I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0_CON
R7716 1 2 22R 5% R0402 — I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0_CON
R7717 1 2 22R 5% R0402 — PA_EN_H_GPIO3_C3
R7719 1 2 22R 5% R0402 — I2C3_SCL_M0

R7720 10K 5% R0402

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK_EVB1_RK3568_DDR4P216SD6		
File:	77.Audio-MIC Array Interface		
Date:	Wednesday, September 23, 2020	Rev:	V1.0
Designed by: Zhangdz	Reviewed by: Default	Sheet:	41 of 50

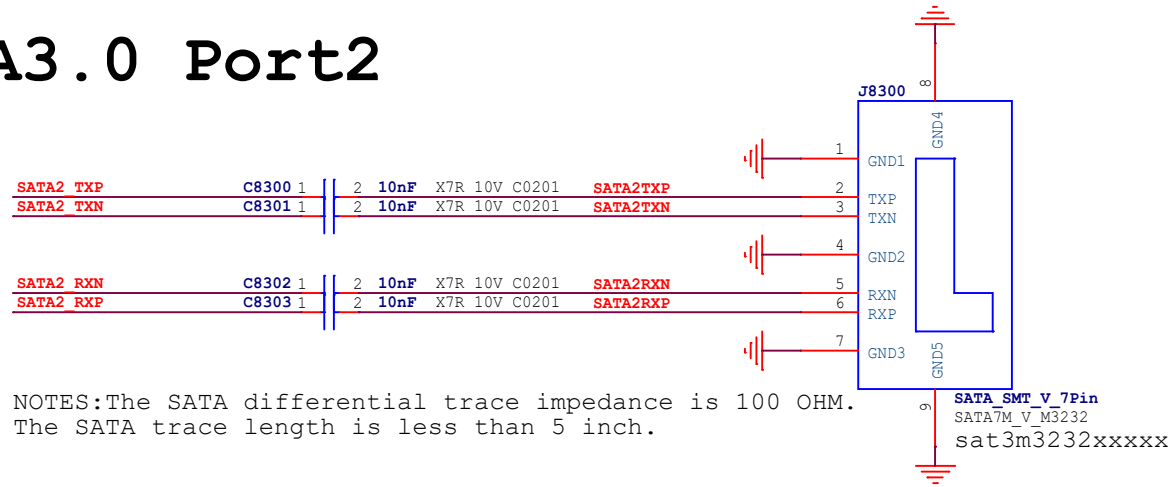
PCIe3.0 x 2Lanes (X 4Slot)



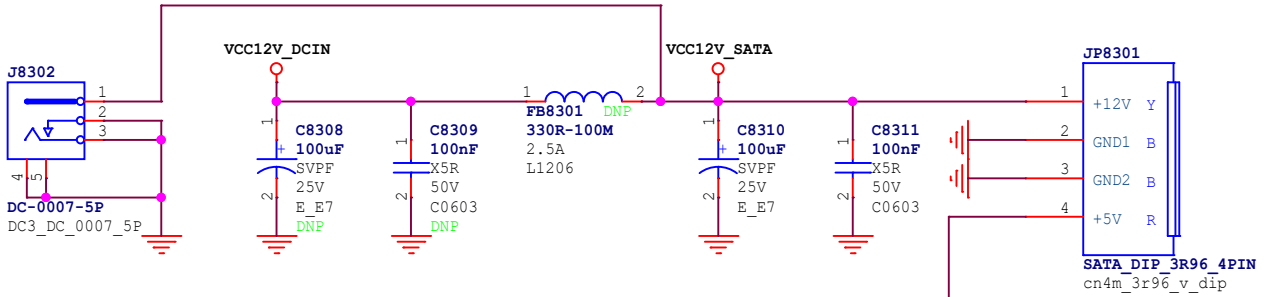
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK_EVB1_RK3568_DDR4P216SD6
File:	82.PCIE-PCIE3.0_Slot
Date:	Wednesday, September 23, 2020
Rev:	V1.0
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	42 of 50

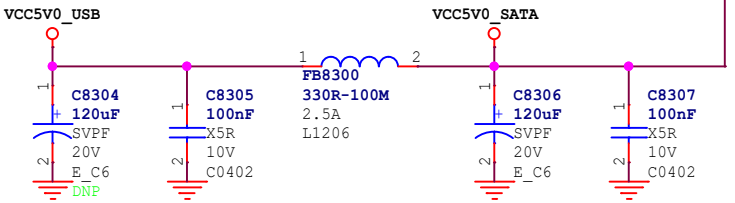
SATA3.0 Port2

SATA2_TXP
SATA2_TXN
SATA2_RXP
SATA2_RXN
SATA2_ACT_LED

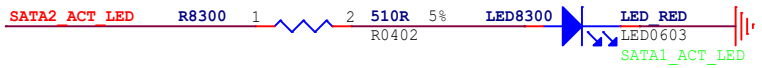


NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.





NOTES:Close to DC Port



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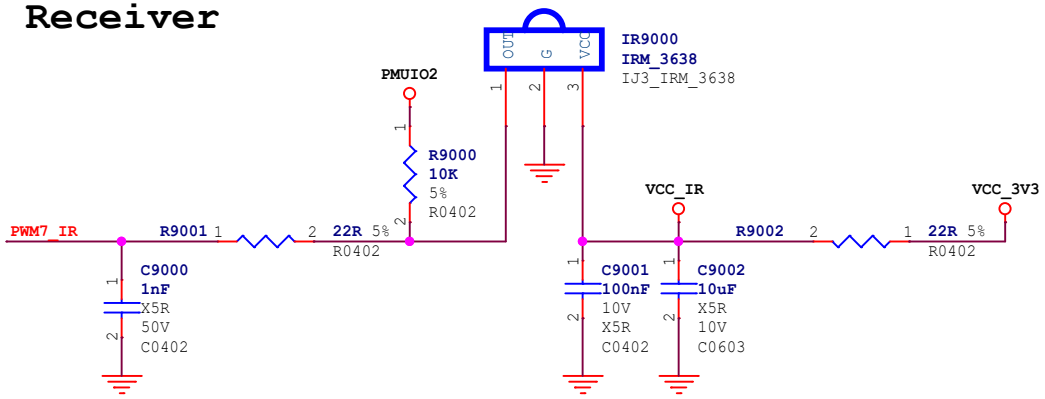
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	83.SATA-SATA3.0 Slot_7P				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	43 of 50

PWM7_IR

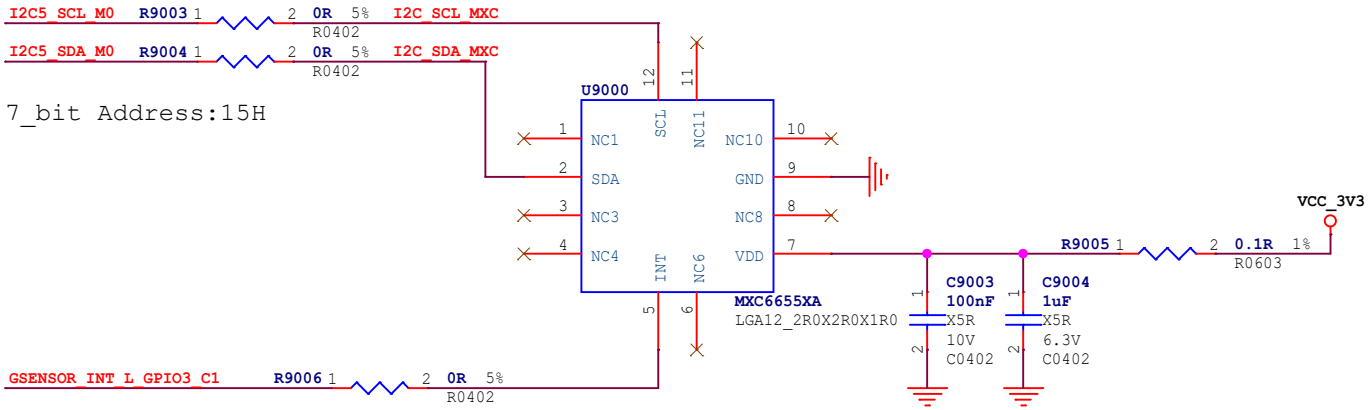
I2C5_SCL_M0
I2C5_SDA_M0

GSENSOR_INT_L_GPIO3_C1

IR Receiver



Gyroscope+G-sensor

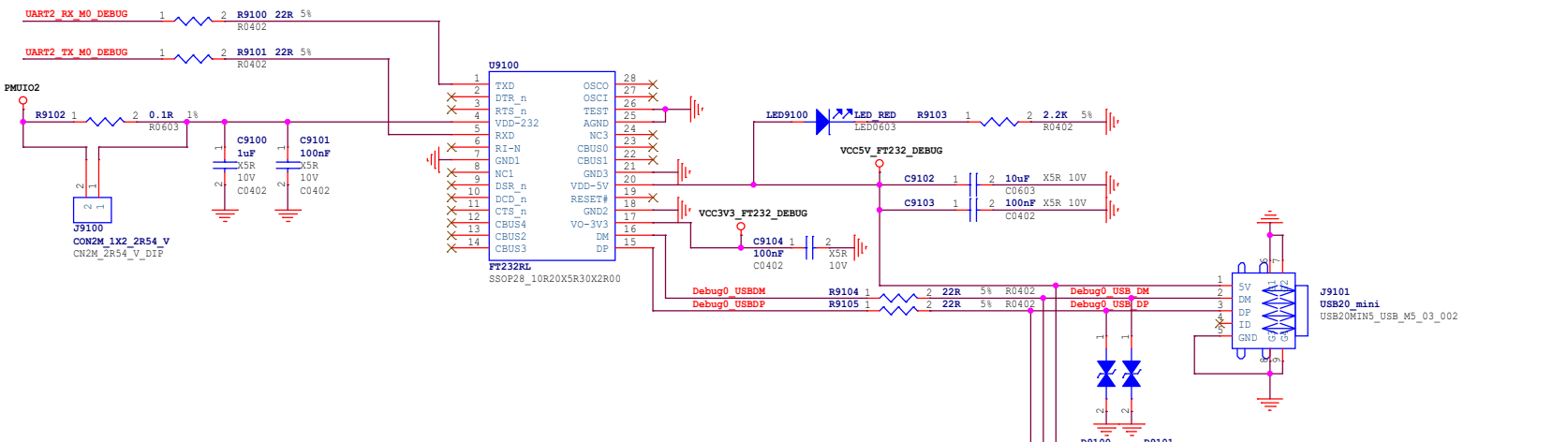


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	90.Sensor/IR Receiver				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	44 of 50

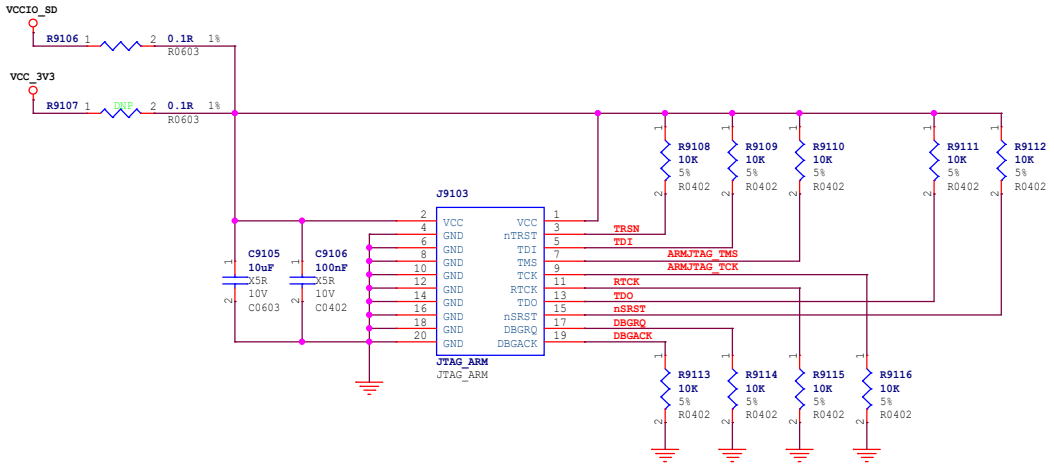
UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

ARMJTAG_TCK
ARMJTAG_TMS

Debug UART2



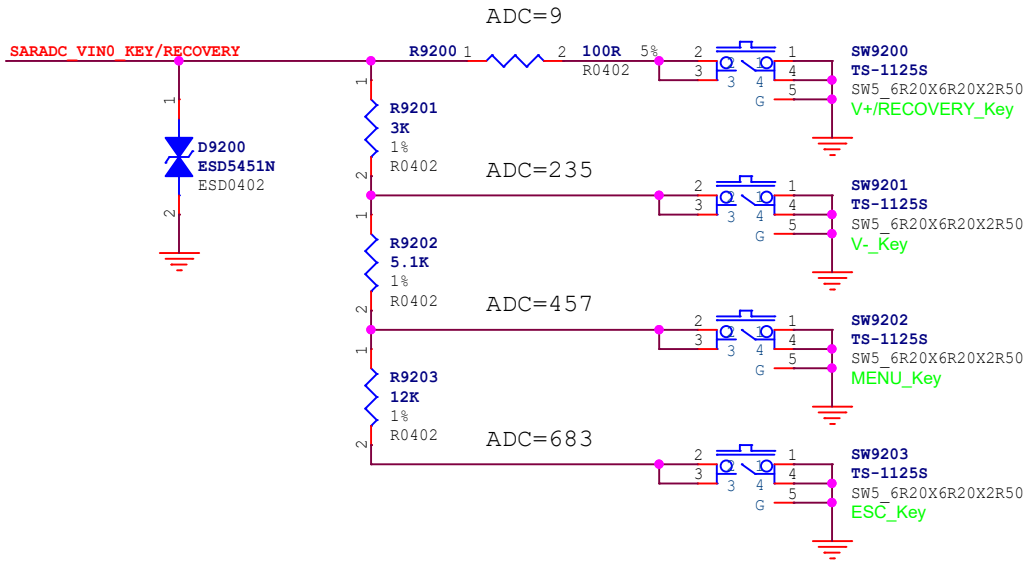
ARM JTAG

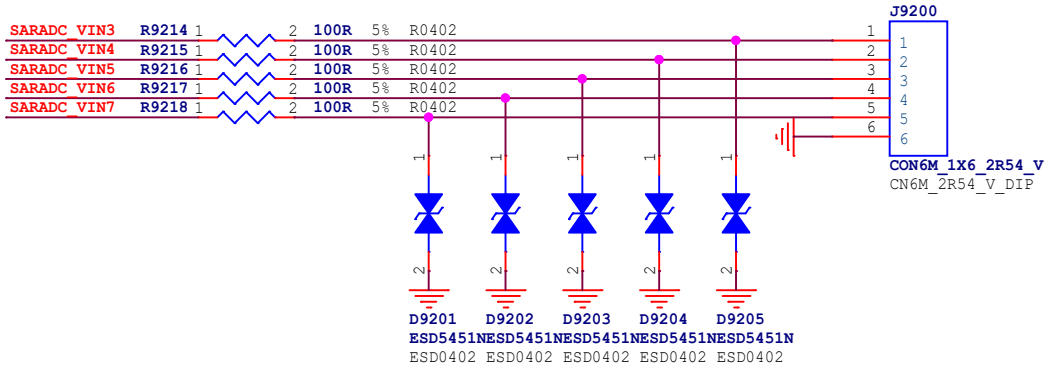


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	91.Debug UART/JTAG Port				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	45 of 50

SARADC_VIN0_KEY/RECOVERY

SARADC_VIN3
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

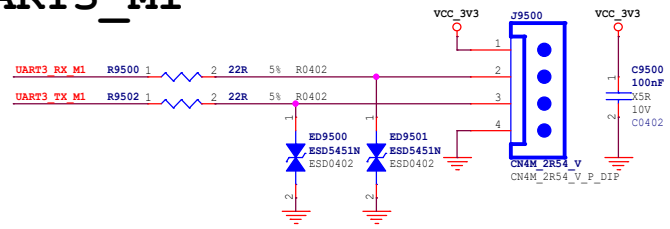




Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	92.KEY Array				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	46 of 50

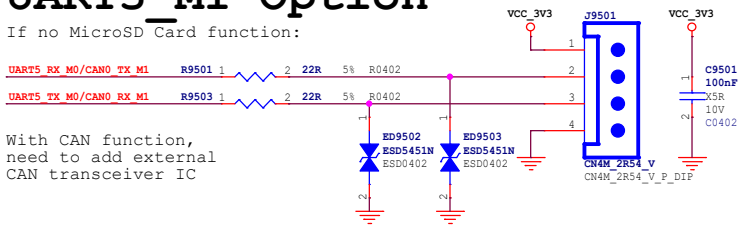
UART4_RX_M1
UART4_TX_M1
UART3_RX_M1
UART3_TX_M1
CAN1_RX_M1
CAN1_TX_M1
UART9_TX_M1
UART9_RX_M1
UART6_TX_M1/PWM8_M1
UART6_RX_M1/PWM9_M1
UART5_RX_M0/CAN0_TX_M1
UART5_TX_M0/CAN0_RX_M1

UART3_M1



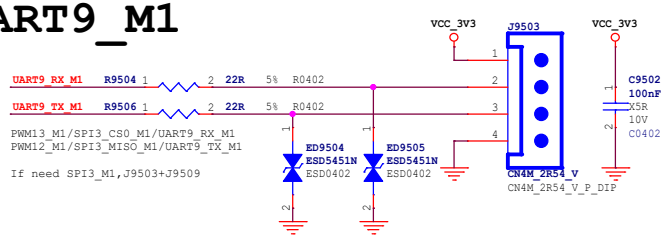
UART5_M1-Option

If no MicroSD Card function:



With CAN function,
need to add external
CAN transceiver IC

UART9_M1

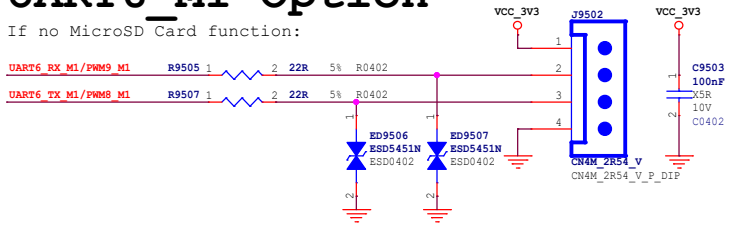


PWM13_M1/SPI3_CS0_M1/UART9_RX_M1
PWM12_M1/SPI3_MISO_M1/UART9_TX_M1

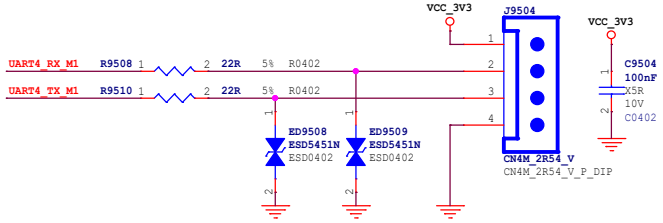
If need SPI3_M1,J9503+J9509

UART6_M1-Option

If no MicroSD Card function:

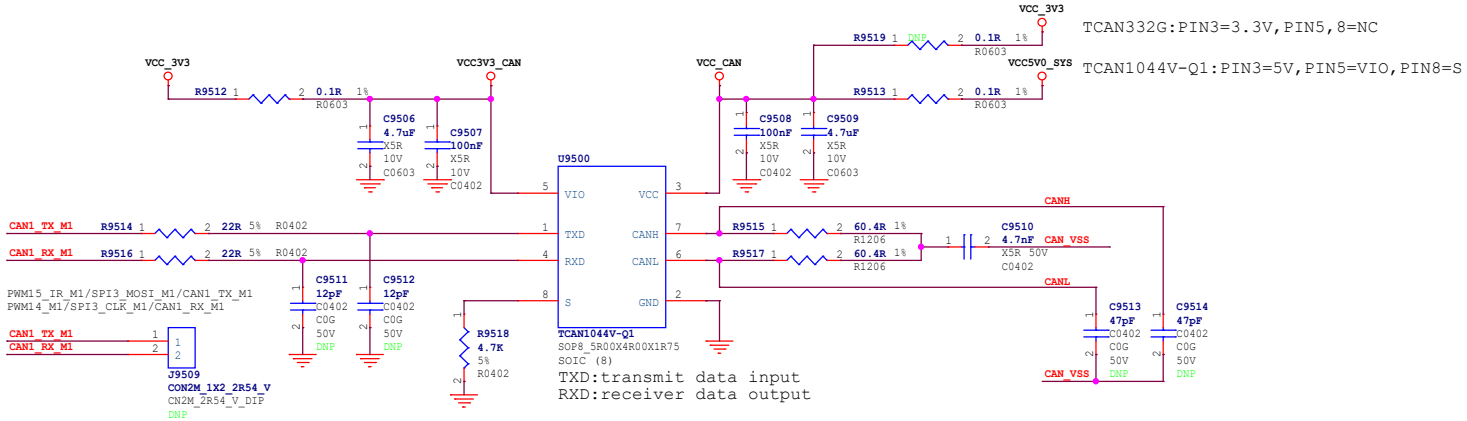


UART4_M1



CAN1_M1

CAN transceiver IC

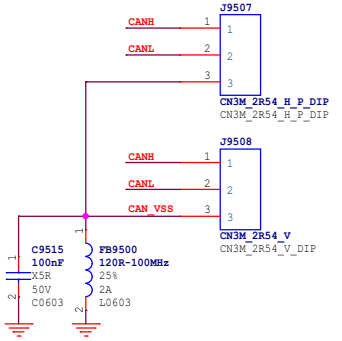


PWM15_IR_M1/SPI3_MOSI_M1/CAN1_TX_M1
PWM14_M1/SPI3_CLK_M1/CAN1_RX_M1

TXD:transmit data input
RXD:receiver data output

TCAN332G:PIN3=3.3V,PIN5,8=NC

TCAN1044V-Q1:PIN3=5V,PIN5=VIO,PIN8=S



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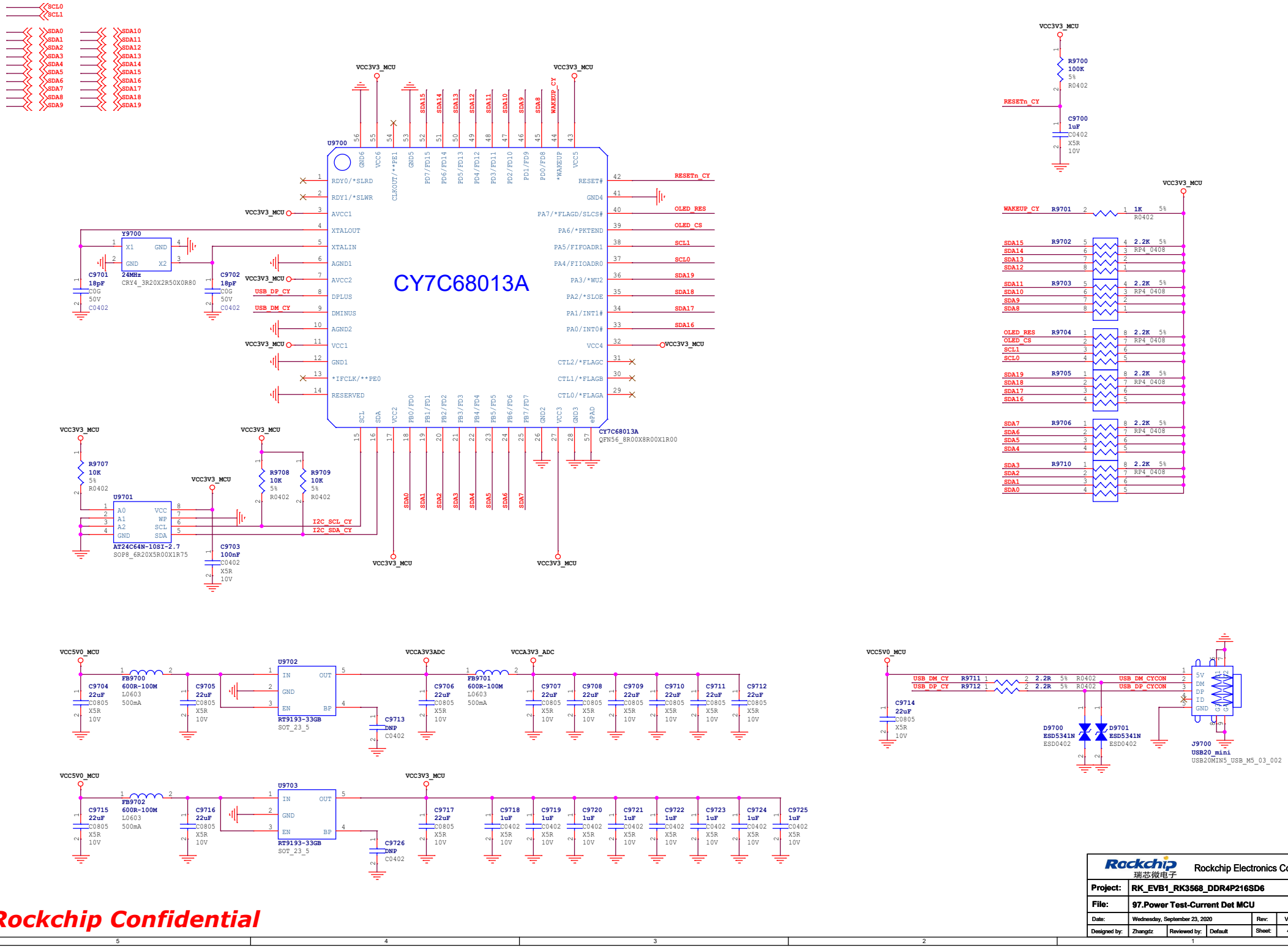
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	95.UART/CAN Port				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	47 of 50



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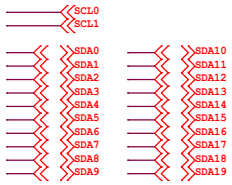
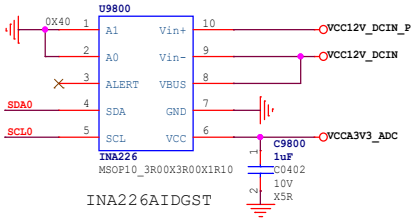
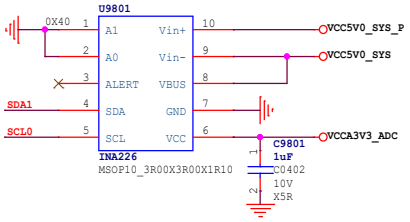
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	97.Power Test-Current Det MCU				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	48 of 50



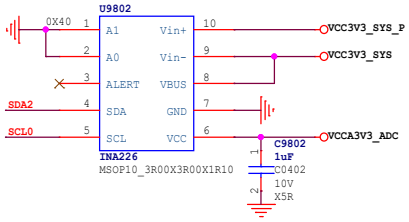
VCC12V_DCIN-0.02R



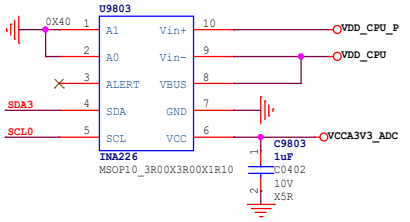
VCC5V0_SYS-0.02R



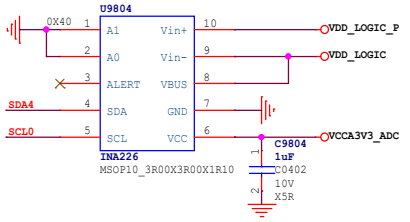
VCC3V3_SYS-0.02R



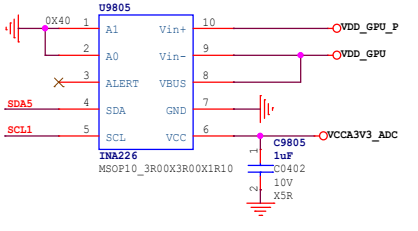
VDD_CPU-0.01R



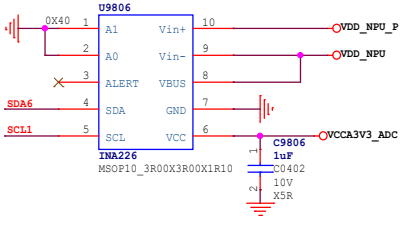
VDD_LOGIC-0.02R



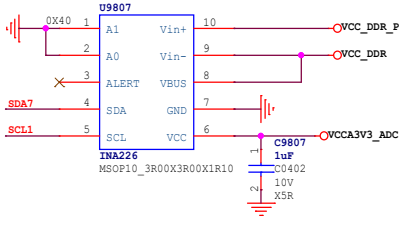
VDD_GPU-0.02R



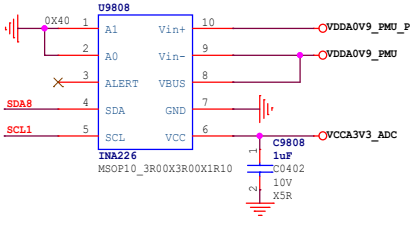
VDD_NPU-0.02R



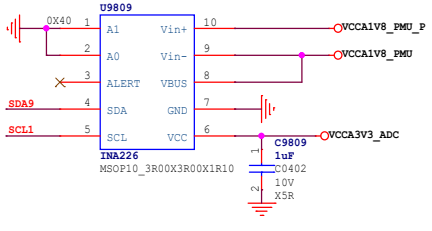
VCC_DDR-0.02R



VDDA0V9_PMU =0.05R



VCCA1V8_PMU=0.05R



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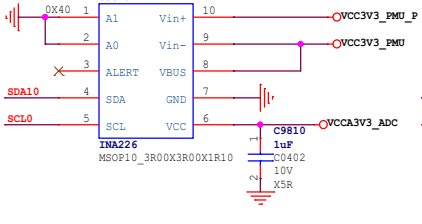

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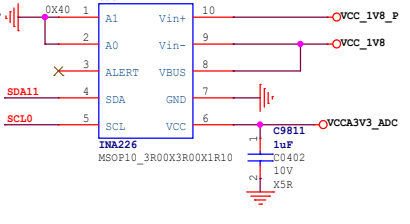

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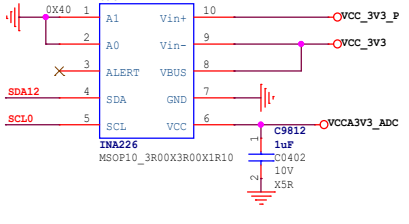

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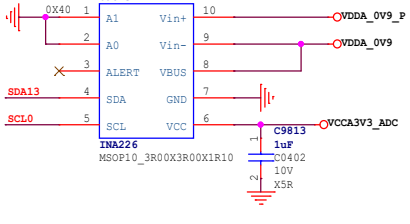
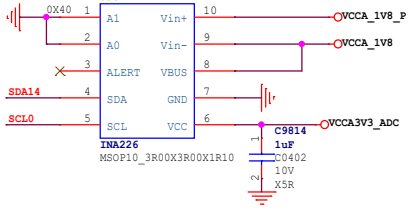
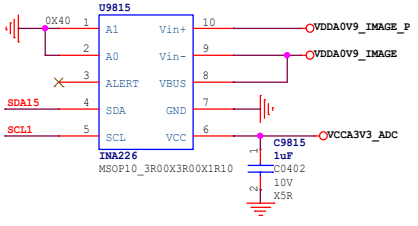


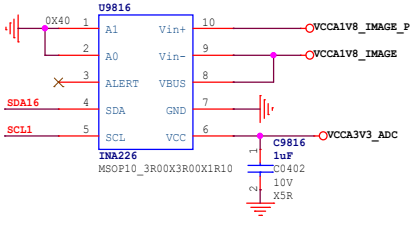
VCCA_1V8 =0.05R



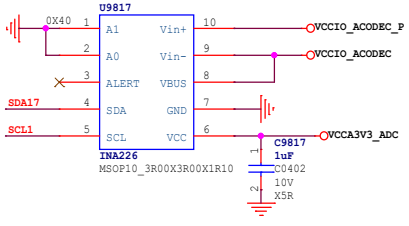
VDDA0V9_IMAGE =0.05R



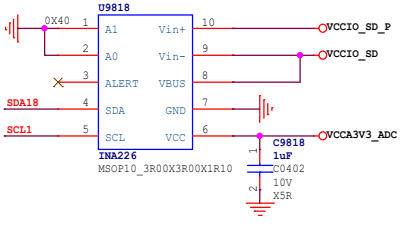
VCCA1V8_IMAGE =0.05R



VCCIO_ACODEC =0.05R



VCCIO_SD=0.05R



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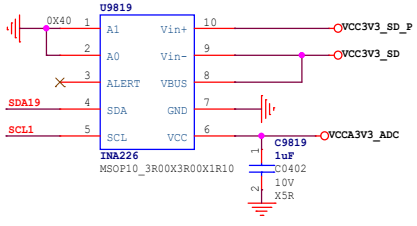

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Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	98.Power Test-ADC				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	49 of 50

H9900 HOLE_3R20 HOLE_C3R20_C6R00
H9901 HOLE_3R20 HOLE_C3R20_C6R00
H9902 HOLE_3R20 HOLE_C3R20_C6R00
H9903 HOLE_3R20 HOLE_C3R20_C6R00
H9904 HOLE_3R20 HOLE_C3R20_C6R00
H9905 HOLE_3R20 HOLE_C3R20_C6R00
H9906 HOLE_3R20 HOLE_C3R20_C6R00
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H9909 HOLE_3R20 HOLE_C3R20_C6R00
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H9915 HOLE_3R20 HOLE_C3R20_C6R00
H9916 HOLE_3R20 HOLE_C3R20_C6R00
H9917 HOLE_3R20 HOLE_C3R20_C6R00
H9918 HOLE_3R20 HOLE_C3R20_C6R00
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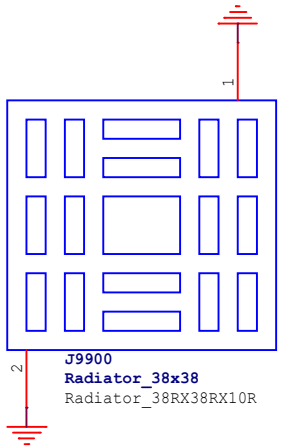

SMTSO9900 SMTSO2050CTJ SMTSO_M2_C3R6_C6R0_L5R0
SMTSO9901 SMTSO2050CTJ SMTSO_M2_C3R6_C6R0_L5R0

GND9900 GND_GATE CON2_1X2_5R08_DIP
GND9901 GND_GATE CON2_1X2_5R08_DIP
GND9902 GND_GATE CON2_1X2_5R08_DIP
GND9903 GND_GATE CON2_1X2_5R08_DIP
GND9904 GND_GATE CON2_1X2_5R08_DIP
GND9905 GND_GATE CON2_1X2_5R08_DIP
GND9906 GND_GATE CON2_1X2_5R08_DIP
GND9907 GND_GATE CON2_1X2_5R08_DIP
GND9908 GND_GATE CON2_1X2_5R08_DIP

TOP Mark

M9900 MARK MARK
M9901 MARK MARK
M9902 MARK MARK

BOTTOM Mark

M9903 MARK MARK
M9904 MARK MARK
M9905 MARK MARK

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK_EVB1_RK3568_DDR4P216SD6				
File:	99.Mark/Hole/Heatsink				
Date:	Wednesday, September 23, 2020			Rev:	V1.0
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	50 of 50